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A possible scheme for the trigger and data acquisition of the FAST detector.

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Abstract.

The Fibre Active Scintillating Target (FAST) is intended for direct muon life time measurements. The FAST detection volume is built of (48 x 48) scintillating fibre units each of 200mm length with 4x4mm^2 cross-section. All the fibre units are arranged parallel to each other and aligned orthogonal to the beam direction. The granularity of the detector allows to identify the stopping point of the primary pion and to detect the appearance of a secondary muon and its decay. The spread of the pion beam over all transverse area of the detector should provide a random distribution of the pion stopping points in the target volume and permit simultaneous registration of about ten events overlapped in time.

A structure of the trigger electronics and data acquisition system for FAST is described. It permits to work with 1MHz mean rate of beam particles, it rejects overlapping events and decreases the rate of raw data down to 30Mbytes/s. The raw event data consist of geometrical and timing information from the 25 pixels surrounding the pion stopping point. The data acquisition system may also perform final processing of the raw data.

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1. Introduction.

The Fiber Active Scintillator Target - project [1] has been proposed to improve the experimental accuracy of the effective weak coupling constant G_F by about one order of magnitude. This could be reached measuring the muon mean lifetime with 20 times better precision than in previous experiments [2,3]. These experiments were in particular limited by the rate of incoming beam particles because the rather long muon lifetime of 2.2 μs leads to an overlap of events in time already for rates of about 100 kHz. To work with a 1 MHz beam particle rate as suggested for FAST needs therefore a well structured target and special care for events overlapping in space and time.

To optimise the target structure we made a corresponding GEANT simulation [4]. Best results were found for a two dimensional geometry using scintillating fiber units of 20cm length with a 4x4 mm^2 cross section. A matrix of 48x48 of such units is arranged perpendicular to a 135MeV/c π^+ beam which is spread in one transverse dimension across the target. Each fiber unit is connected to one pixel of a 16 channel Hamamatsu photomultiplier R5900-M16. That needs in total 144 of these PM's where three of them are connected to one target column. Such an arrangement has the clear advantage, that most often only one pixel of a photomultiplier is hit by light from a throughgoing pion.

We simulated 10^5 pion decays for the configuration described. A typical hit pattern of an event is shown in fig. 1. It takes about 0.5 ns for the pion to stop in the middle of the target after crossing on average 25 fiber cells. As can be seen from fig.2 it changes it's original direction in 95 % of all cases by no more than ±2 target rows. With a mean lifetime of 26 ns the pion decays at the stopping point giving rise to a muon. The muon stops in the same fiber unit or in an adjacent one as can be seen from figs.3a and 3b. It then decays after on average 2.2 μs producing a positron which can be observed again in the direct neighbourhood of the muon stopping point (see figs.3c and 3d). The positron crosses many fiber units and rather often even leaves the target.

In fig. 4 the number of photo-electrons expected to be observed from the fiber cells of the stopping π^+ , the stopping muon and the appearing positron are distributed. The normalisation has been done with respect to minimum ionising particles crossing 1 mm blue fibers producing photons seen by a bialcali photocathode. As can be seen a lot of light is produced by the stopping π^+ and μ^+ whereas the positron yields a considerably smaller number of photo-electrons . So the front end electronics has to take into account a large dynamic range of signals.

2. Trigger and data acquisition (an idea).

The typical event in FAST may be described as follows. In the three dimensional space (x,y,t) hits of the primary pion, secondary muon and positron build up three separated tracks having small curvature. These tracks are concatenated into a single curve in the two-dimensional space (x,y). The gaps between these three tracks in the direction of the time-axis (t) are equal to the life time of the pion and muon. Such an event represents the $\mu-\nu$ decay of the pion at rest and consecutive $e-\nu-\nu$ decay of the muon at rest. Background events arise due to several reasons. First, the event data may be polluted by single noise hits or even by tracks of a positron belonging to another $\pi\to\mu\to e$ event. Second, the pion may decay in flight giving rise to a two- or a three-track-event with a quite long muon track. And third, a rare $e-\nu$ decay of the pion causes two concatenated tracks.

The proposed trigger system finds the stopping point of the pion and checks whether the event is clean enough or spoiled by other pions, which entered the target until the secondary muon surely decays. As shown in Appendix A, the time period of ≈20μs equal to nine muon mean lifetimes should be considered. The idea of the trigger is to make two snapshots of the event. The exposure time of the first snapshot starts at the entrance time t(0) of the pion into the detector and covers the time up to the pion stops. It must be as short as possible but longer than the time necessary to stop the pion (0.5ns). This first snapshot gives a graphical representation of the pion track. The exposure time of the second snapshot starts as soon as possible after the pion stops and lasts up to the time when the pion surely decays (e.g. ≈240ns equal to nine pion mean lifetimes). The second snapshot contains hits of the secondary muon, in a small fraction of events it samples hits of the descendant positron as well. The trigger system recognises the event as a decay of the pion, when the end of the pion track in the first snapshot coincides in (x,y) space with the beginning of a secondary track in the second snapshot.

This coincidence point is taken as the stopping point of the pion t(0). The trigger system checks whether the event t(0) is superimposed by any other event arriving in the time interval [t(0)-20µs, t(0)+20µs]. If there are no other pions in the vicinity of the stopping point, the trigger is fired and the TDC's of the data acquisition system measuring the hit time within a small window around the pion stopping point are triggered. If not, the pion at t(0) is rejected.

The data acquisition system reads the triggered TDC's and takes only hits within the time interval [t(0), t(0)+20µs]. These data consist of hits of the pion t(0), its descendants (muon and positron) and may be polluted by tracks of other pions or their decays. The data acquisition system is equipped with digital signal processor boards, performing on-line recognition of the muon and positron hits and extracting timing information of the muon and pion decays.

For control and monitoring purposes the trigger and data acquisition system should allow to read out the list of the stopping points and hits from all TDC's falling into the search window of 20µs.

3. The trigger electronics.

The detection volume (48x48 fiber units) of the FAST is divided into two parts. The first two front layers are dedicated for first level triggering. The rest of the volume is used in second level triggering and for time measurements. Light from scintillating fiber units is detected by PM's, amplified and fed to time-discriminators, delivering output signals with minimal time-jitter. The precision necessary for the time measurements is discussed in Appendix A.

The first level trigger detects coincidence of signals in the two front layers and delivers the pion entry point (Y_entry) to the second level trigger (fig.5). The fiber units of the main volume of the target are arranged row-wise for the triggering and time measurements. All cells of each row are processed by an associated bitmap unit. The trigger electronics consists of the 48 bitmap units and 2LvlTrigger processor and occupies a trigger crate. The bitmap unit contains a 46-bit wide pipeline clocked by 100MHz providing a time delay of hits equal to the decision time of the first level trigger, and two registers. If a pion enters the target at time t(0), the bitmap units of five rows around the entry point are activated and the D-registers sample hits in the time window [t(0),t(0)+10ns] whereas the RS-registers collect hits in the time interval [t(0)+10ns,t(0)+240ns]. The pion entry point is written to the 2LvlTrigger processor as well. During the subsequent 240ns period the activated bitmap units can't be used for the registration of a further pion. If a next pion enters the target too close to the previous pion and their sections of the target are overlapped, the next pion entry is accompanied with a 'spoiled' flag. Such a 'spoiled' entry point has no effect on bitmap units, it doesn't activate them, it's only passed to the 2LvlTrigger.

The aim of the 2LvlTrigger processor is the identification of the pion stopping point and check whether another pion stops in the neighbourhood (5x5) around it. The 2LvlTrigger (fig.6) writes the entry point together with the 'spoiled' flag and a rough time-stamp to the input FIFO_A. The bus controller takes an entry point from the FIFO_A, pushes it to the intermediate FIFO_B and in the case of a 'clean' event it starts reading snapshots from the five bitmap units associated with the pion stopping point. Processing of the snapshots is performed by the tracker (fig.7) implemented in a FPGA. The snapshots are read from the data FIFO_C in a row-wise manner to the register bank of the tracker and processed by shifting the snapshots column-wise in the up-beam direction and checking whether the end of the pion track is reached or not. The end-of-pion-track condition is satisfied when there are no continuation of the pion track in the first snapshot and there is a hit in the nearest neighbourhood in the second snapshot. If it is the case, a stopping point of the pion is identified and its position (Xs,Ys) along with the rough time stamp and the flag is pushed to the FIFO_D. If the check fails, the corresponding pion entry point is removed from the intermediate FIFO_B. The tracker can be clocked with 50MHz. That leads to a processing time of the snapshots of the order of 500ns.

The list processor (fig.8) has to check whether the event t(0) is superimposed by any other event arriving in the time interval [t(0)-20μs,t(0)+20μs]. For that the list processor stores the list of events in a register bank organised as a list of entries. Each entry contains a pion stopping point with the rough time-stamp and the flag 'spoiled/clean'. The list of events is written from the top, writing of the latest event shifts all the previous down to the bottom of the list. The list processor constantly compares the time-stamp of an event at the bottom of the list with the current time value, taken from the coarse timer. If the difference is smaller than 20μs and the FIFO_D keeping a queue of pion stopping points is not empty, it takes from the FIFO_D the next event and writes it on top of the list. When the difference exceeds 20μs, the list processor compares the pion t(0) stopping point, which is at the bottom of the list with all other events in the list. If no event is found in the vicinity of the pion t(0) stopping point, the event t(0) is accepted, the stopping point (Xs,Ys) is removed from the list and sent to the data acquisition system to trigger the TDC's associated with this stopping point. If the list processor finds an event t(i) which is too close to the event t(0), it marks the event t(i) as 'spoiled', rejects the event t(0) and removes it from the list. The 'spoiled' event is kept in the list until it reaches the bottom of it, it can't fire the trigger of TDC's, but it can spoil other events. An implementation of the described list processor seems to be feasible using a Xilinx FPGA of type XC6200 [5]. It allows to keep the event list processing time below 500ns.

4. The data acquisition system.

A sketch of the data acquisition system is presented in fig.9. It consists of 48 multi-channel TDC modules, occupying three VME crates, and three SHARC [6] based VME processor-modules. Each TDC is associated with a row of fiber units of the target and measures the time of the hit signals of this row. Let's consider the implementation of the TDC modules based on the state of the art TDC-chip, developed by the CERN/ECP-MIC Division [7]. This TDC-chip is a 32-channel multi-hit TDC. It has an internal circular hit-buffer and a special trigger channel, giving a reference time t(tr). The user is able to define which time interval with respect to this reference is interesting to him. In our case, we wish to read hits from the time interval [t(tr)-20μs, t(tr)] . The TDC-chip organises itself reading the hit buffer. It stores the hits falling into the time interval in an internal event FIFO and skips events which are outside the time interval. Unfortunately there is no way to take from the hit buffer only hits of certain channels of the TDC. The TDC chip reads hits of all the channels from the assigned time interval including hits outside the neighbourhood (5x5) of the pion stopping point, but at the same time it doesn't remove from the buffer hits belonging to other events. That can overload the VME data transfer bus. To keep the data rate on the VME-bus low, the TDC module (fig.10) is equipped with a skip logic, which reads hit data associated with the trigger and stores only hits from the pion stopping point neighbourhood in the event FIFO.

Each multi-SHARC VME processor-module of the data acquisition system receives the y-coordinate of the pion stopping point from the second level trigger. For that a Link port (or Serial port) of a SHARC processor may be used. The processor module checks whether the section of the target, for which it is responsible, contains all event information, part of it or the event is displaced fully in another VME-crate of the data acquisition system. In the first case the module reads the event data via its VME-bus. In the second case it collects part of the data via the VME-bus and sends this part to an adjacent processing module (or receives another part of the data from it, depending on the assigned order). In the last case the processor module doesn't perform any action, it just skips the stopping point in question. When a complete event is collected in the module, it may be processed by the SHARC processors and the time interval between the stopping point of the pion and the first hit of the muon may be calculated. The raw data as well can be delivered to the outer world for their storage or/and monitoring of the detector. The mean rate of the raw data from each processor module is of the order of 10Mbytes/s.

5. Dead time and data flows.

The timing of the trigger and data acquisition system is summarised in the table.1. The dead time of the system is determined by the time taken by bitmap units for creating the snapshots of an event. Only nine rows of the detector (five rows of fiber units covering the event, and four nearest rows joining the activated corridor, two at each side) are blocked for 240ns after the pion enters the target. Since reading the snapshots of an event out of the bitmap takes a longer time (~1µs), each bitmap unit is equipped with a FIFO (hidden inside the bus-interface on fig.6), which samples the snapshots immediately after 240ns 'exposure' period and allows to start the accumulation of the next snapshots without additional delay. At an average pion rate of 1MHz this decreases the detection efficiency by 4.5%.

The time windows of accumulating two snapshots have influence on the efficiency of the system. The data acquisition system has to measure only hits of an event where the last pion and first muon signals are clearly separated in time. These two signals in fact identify the stopping point of a pion. Due to the digital delay of the bitmap unit clocked with 100MHz the time-resolution of the trigger system is limited to 10ns, giving a reduction of the detection efficiency to about 70%. The trigger system allows to avoid the reduction of the efficiency, if a softer identification condition for the pion stopping point is selected: e.g. the rightmost end of the primary pion track may be taken as the stopping point of the pion (the snapshot collected in time interval [t(0)+10ns,t(0)+240ns] is not used in this case).

Processing of the events in the 2LvlTrigger module is organised as a pipeline. First, an event is read via the backplane-bus of the trigger crate. Then it is processed by the tracker. And later it is analysed by the List processor. The throughput of the 2LvlTrigger processor is determined by the slowest of these three processes, particularly by reading the bitmap units. The 2LvlTrigger processor has to read the snapshots of an event in 1µs, it has to collect them from 5 different bitmap units. This requires a throughput of the trigger crate bus of up to 60MB/s in a 'single-word' transfer mode. The standard VME bus can't operate with such a data rate. One of the possible solutions is to restrict the VME protocol in the trigger crate to the A16 addressing mode and to extend the data bus width to 48-bit at the expense of 16 most significant bits of the VME address bus. This will allow to decrease the cost of trigger electronics (usage of a standard VME-crate and low cost of interfacing).

When the trigger conditions are satisfied, TDC's digitising hits from 5 rows of the target, covering the pion stopping point are triggered. It happens ~20µs after the pion entered the target. Each 32-channel TDC chip has a limited depth of a hit memory equal to 256 words. That means the total amount of hits in 32 pixels of each row during the time interval of 20µs must not exceed 256, this condition will be always fulfilled. After triggering the TDC chip, it needs some time to perform the search for hits belonging to the trigger (trigger latency time 20µs, trigger window 0). In the worst case one has to scan through the whole buffer, it may take up to 6.4µs. Different hit densities in the different rows leads to varying processing times and the data in the event FIFO's of the TDC's will not be ready simultaneously. The SHARC-board has to read out the TDC modules after a certain delay with respect to the triggering of the TDC's. The delay must be in the range of 7µs to guarantee readiness of the event data. The data should be accompanied by an event header, encoding the position of the stopping point and the number of hits belonging to the event. In total the SHARC-board has to read via VME-bus 5 headers and up to 10 hits per event.

Appendix. A. Interval of time measurements and time-jitter.

As a result of the FAST experiment we will get the histogram $\{\ln N_i, t_i\}$, where N_i is the total number of events with the time difference between the muon and positron signals equal to t_i. The mean life time of the muon τ_μ will be found from the least-square approximation of the histogram with a straight line. Precision of the estimated value of the muon mean life time is determined by a total number of collected events N_Σ , maximum and minimum times (T_{max} , t_{min}) detectable by the data acquisition system and the accuracy σ_t of individual time measurements. The experimental data $\{\ln N_i, t_i\}$ carry uncertainty in both variables. Since N_i obeys the Poisson distribution, the RMS deviation of $\ln N_i$ is equal to $N_i^{-1/2}$. One can regard the pair $(\ln N_i, t_i)$ as an event composed of N_i independent events, each representing the time interval between the muon and positron signals equal to t_i with uncertainty σ_t. Therefore the error of t_i is $N_i^{1/2}$ times smaller than the RMS error σ_t of the individual time measurements. Analysis of the errors of the least-squares parameter estimation becomes quite simple for the case when one of the variables is known precisely [8]. Assuming the t_i are known without error, one can derive for the error in mean-life time

$$(\sigma_\tau)_{(N)} \approx \frac{\tau_\mu}{\sqrt{N_\Sigma}} * \frac{1}{\sqrt{1-\frac{\alpha^2 e^\alpha}{\left(e^\alpha - 1\right)^2}}} \quad , \tag{A.1}$$

where $\alpha = (T_{max} - t_{min})/ \tau_\mu$.

If the $\ln N_i$ values have no uncertainty, the mean-life time error may be expressed as

$$(\sigma_\tau)_{(t)} \approx \frac{\sigma_t}{\sqrt{N_\Sigma}} * \frac{1}{\sqrt{1-\frac{\alpha^2 e^\alpha}{\left(e^\alpha - 1\right)^2}}} \tag{A.2}$$

Both formulas were derived assuming that the TDC resolution (determined by the value of the least significant bit LSB of the TDC) is considerably smaller than the muon mean life time τ_μ .

From these formulas we can conclude the following.

1. The time-measurements may be regarded to be precise, when $\sigma_t \ll \tau_\mu$.
2. The LSB contributes to σ_t and it must also fulfil the condition LSB $\ll \tau_\mu$.
3. The wider the interval of time measurements ($T_{max} - t_{min}$) , the smaller is the total amount of events necessary to reach the same accuracy of the mean life time.
   The effect of the interval width on the accuracy of the mean lifetime can be neglected, if it's wider than 9 * τ_μ .
4. Due to the exponential decay law the minimum measurable time t_{min} greatly influences the number of recordable events.

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Table1. Timing and data rates of the trigger and data acquisition system.

Procedure	Time consumption	Dead time.	Data flow (I)
1st level trigger (coincidence and discriminators)	≈30ns	10ns	
Bitmaps creating	240ns	270ns	
2nd level trigger			
- read the bitmaps	1µs		60 MB/s
- load the tracker	200ns		
- find a stopping point	500ns		
- load the list processor	50ns		
- process the list of events	500ns		
TDC modules		<10ns	
- scan internal hit buffer	< 6.4µs		
- take data to the skip logic	25ns/hit		
- put data to the event FIFO	25ns/hit		
Data acquisition processor			≈15MB/s III)
- read event headers	5*100ns		
- read the event from TDC's	100ns/hit		
- receive part of the event from another processor	75ns/hit +200ns (IV)		

(I) At 1MHz rate of the primary pions.
(II) Assuming at maximum 25 hits in a TDC in one event, no more than 5 of the hits fall into the neighbourhood (5x5).
(III) At maximum the event consists of 10 hits in the (5x5) window and 5 headers.
(IV) Four clock cycles of the SHARC are necessary to respond to an interrupt, additional time is taken also for the link activation.