

A MCM-D-type Module for the ATLAS Pixel Detector

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Abstract

For the ATLAS experiment at the planned Large Hadron Collider LHC at CERN hybrid pixel detectors are being built as innermost layers of the inner tracking detector system. Modules are the basic building blocks of the ATLAS pixel detector. A module consists of a sensor tile with an active area of 16.4 mm x 60.4 mm, 16 read out IC's, each serving 24 x 160 pixel unit cells, a module controller chip, an optical transceiver and the local signal interconnection and power distribution busses. The dies are attached by flip-chip assembly to the sensor diodes and the local busses.

In the following a module based on MCM-D technology will be discussed and prototype results will be presented.

I. GENERAL CONSIDERATIONS

For easy module interconnections, the data lines, control lines, and power distributions are in this scheme routed to the periphery of the module, to a module controller chip and a power distribution cable. All electronic chips are located in the same plane. To avoid complicated wiring and different interconnection technologies, all lines in this proposal are deposited directly onto the detector substrate. The interconnection lines are thus located between the sensor silicon and the electronic chips. Such a module can be made using multi-chip module (MCM) technology. Figure 1 shows a proposed module with outer dimensions of 21.4 x 67.8 mm².

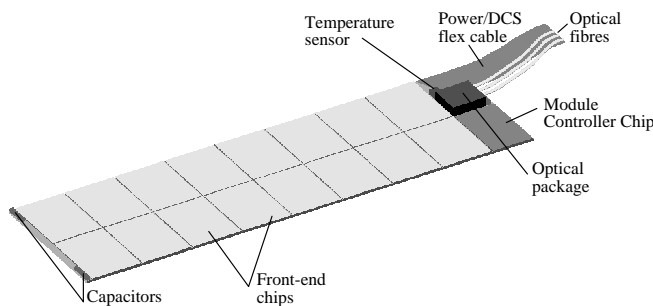


Figure 1: Proposed multi-chip module.

The type of technology proposed is called MCM-D as the chip interconnections are formed by *depositing* dielectric materials and conductors onto a base substrate. In our case it is high-resistivity, active, fully depleted silicon. The production technology closely follows semiconductor techniques. The most commonly used conductor materials are aluminum, cop-

per, or gold. Dielectric materials might be silica, polyimide, or benzocyclobutene (BCB) with a thickness of about 3 to 25 μm . Photolithography, sputtering, electroplating, wet and dry etching are used to create the interconnections. The focus of the MCM-D technology is to achieve high integration density with good frequency behavior in a cost effective process.

In the LHC environment we have to deal with "medium" frequencies. But even for clock rates of 40 MHz one has to take care that line capacitances and line resistances do not cause RC-line charging which may slow down signal speeds quite considerably. In the higher frequency domain the interconnections must be controlled-impedance transmission lines and should be terminated. The line cross sections have to be "large" to decrease dc and ac resistive losses. The power and ground plane positioning in the layer stack becomes important. A structure which is favorable for our application is a microstrip line configuration where the x- and y-signal lines are imbedded into a dielectric material with reference metal planes on top and/or bottom of the structure. In such a MCM-D structure it is possible to build a bus system with low cross talk between two parallel lines with fixed line width, thickness, and line spacing.

For the ATLAS module a four Cu layer system for a signal and power bus is situated below the end-of-column logic of the front end (FE) chips within the outermost 2 mm on both long sides of the sensor substrate. A cross section of the 2 mm wide bus region is sketched in Figure 2. For copper lines of width $w = 20 \mu\text{m}$, thickness $t = 2.2 \mu\text{m}$, with a line spacing $s = 30 \mu\text{m}$, a BCB dielectric medium with $\epsilon_r = 2.7$ and thickness $h = 8 \mu\text{m}$ one computes for a microstrip line configuration a typical line capacitance of 1.2 pF/cm with a time of flight of about 55 psec/cm. The characteristic impedance is $Z_0 \approx 50 \Omega$ and the voltage coupling to the neighbored line is estimated to be -20 dB. For a 7 cm long line the signal attenuation is about 30 % [1].

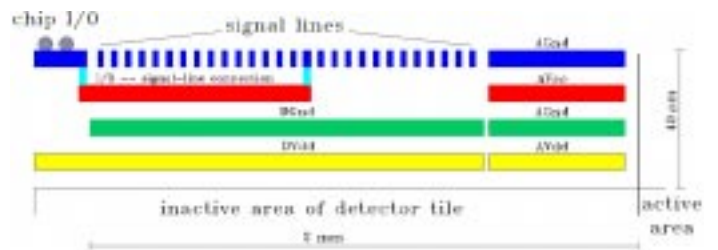


Figure 2: Cross section through the 2 mm wide bus region.

A first try towards a multi-chip module with integrated bus structure for a pixel detector has been carried out for the Very Forward Detector for DELPHI [2]. Ref. [3] describes in some detail mechanical, thermal, and electrical considerations. MCM packaging technology is described in [4].

II. MCM-D PROTOTYPE PROGRAM

To qualify such a technology for ATLAS, co-operative research work has been set up in a prototype program with two independent research and development centers IMEC in Leuven (Belgium) and the Fraunhofer Institute for Reliability and Microintegration IZM in Berlin (Germany).

A. Electrical Characterization

Together with IMEC a first MCM-D prototype has been developed. The substrate was a 4 inch diameter silicon wafer onto which 4 copper layers and intermediate BCB dielectric layers had been deposited. The parameters used were the same as those for the above mentioned calculations. Different test structures were implemented to determine the electrical properties of the bus lines and the optimal structures for the interconnectivity needed for the ATLAS pixel modules. The design of these test structures for evaluation was a necessary first step in the design process due to the high demanding geometrical and electrical specifications of the interconnections on the detector.

With this prototype project possible design rules have been studied. At first the resistive and capacitive characteristics of various types of via connections have been evaluated. These via connections realize the link between the silicon pixel cells and the flip-chip contact pad. The various types of via connections that have been investigated may be classified in two basic types, staggered and staircase, which are both shown in Figure 3.

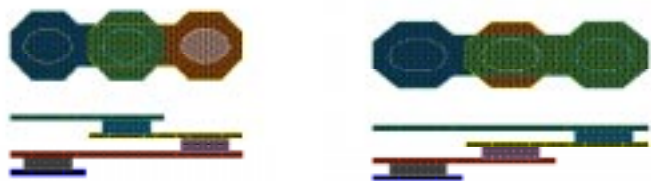


Figure 3: Principle via connection test structures (left : staggered type, right : staircase type).

Using four point measurements, average series resistances of about 80 m Ω and 140 m Ω have been measured for the staggered and staircase type respectively. The average capacitive coupling between adjacent via structures, which are only 50 μm apart, is about 30 fF. The results show that it is possible to build a MCM even with more than 6000 I/O's per cm² from the Si-substrate through the deposited BCB/Cu sandwich to the top metal, the component layer.

The high frequency electrical characteristics of the 7 cm long MCM-D interconnections have been determined using microstrip transmission line test structures. These structures, of which layout sections are shown in Figure 4, have been measured using a HP 8510C network analyzer.

The measurement results indicated that in this case a characteristic impedance of 50 Ω may be realized with 28 μm wide microstrip lines. The lines of the bus test structure are 20 μm wide, and hence a characteristic impedance higher than 50 Ω , namely 67 Ω , has been obtained. The attenuation and cross talk levels along these very long and closely spaced bus lines are very low. Figure 5 depicts a comparison between an active and a coupled bus line. A signal attenuation of 4 dB and a far end cross talk level of maximum 2 % for a fast step signal of less than 100 psec rise time have been measured.

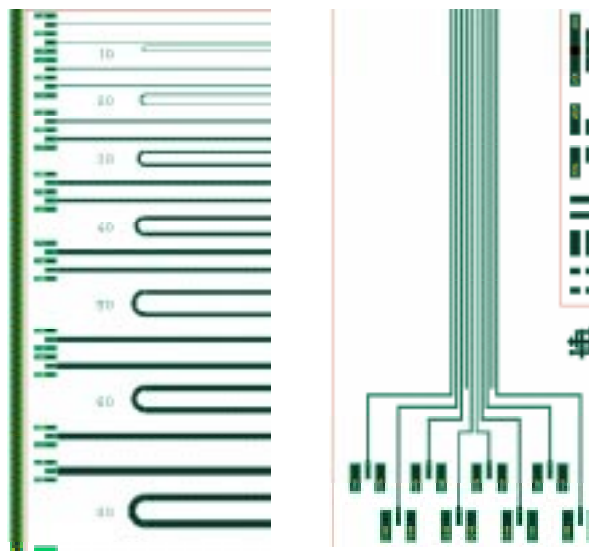


Figure 4: Partial views of the microstrip test structures for the electrical characterization of the MCM-D technology (left: microstrip lines with different line widths (10 to 100 μm), right: 7 cm long bus structure).

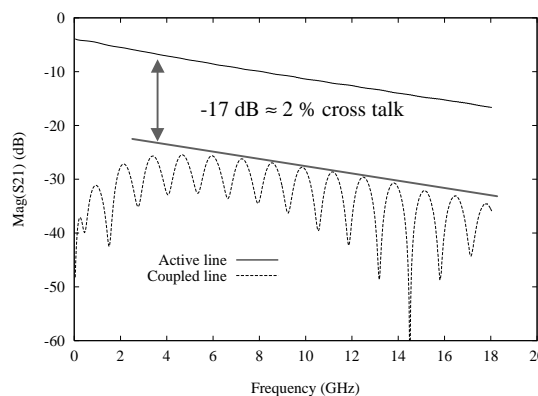


Figure 5: Typical network analyzer measurement results (S21 transmission scattering parameters) for a long active bus structure line and its coupled neighbor (spacing 20 μm). The measured maximum far end cross talk is -17 dB or less than 2 %.

B. Irradiation Tests

As the detector elements are located very near to the circulating beams, all components have to be radiation tolerant enough to survive the expected detector life time. Therefore in a next

step the influence of irradiating the samples with 10^{15} (40 keV) electrons/cm² and with $5 \cdot 10^{14}$ high energy protons/cm² has been investigated. Besides the change in electrical characteristics (e.g. attenuation and capacitive coupling), possible degradation of the BCB dielectric material has been examined by analyzing the effective relative permittivity (ϵ_{r_eff}). From network analyzer measurements of the microstrip transmission lines before and after irradiation, the change in effective relative permittivity may be determined. This is because the difference in frequency at which the phase of the electromagnetic wave propagating along the transmission line reaches a given value (e.g. -180°), is a measure for the difference in effective relative permittivity. For a situation before (index 1) and after (index 2) radiation, the signal phase shift Θ due to radiation may be written as :

$$\Theta = \frac{\omega_1 L}{c_o} \sqrt{\epsilon_{r_eff1}} = \frac{\omega_2 L}{c_o} \sqrt{\epsilon_{r_eff2}} \quad (1)$$

with $\omega_i = 2 \pi f_i$ and f_i the frequency at the reference phase, L the length of the line and c_o the speed of light in vacuum. Rearranging of (1) gives :

$$\frac{\epsilon_{r_eff1}}{\epsilon_{r_eff2}} = \left| \frac{f_2}{f_1} \right|^2 \quad \text{or} \quad \epsilon_{r_eff2} = \epsilon_{r_eff1} \left| \frac{f_1}{f_2} \right|^2 \quad (2)$$

Using this technique, effective relative permittivity changes of about 1.5 % to 2.5 %, depending on the sample, have been measured for both the electron and proton irradiated wafers. Since these values are of the same order of magnitude as the changes in permittivity that may be expected due to moisture absorption in the BCB and measurement tolerances, it may be concluded that the material has not degraded significantly due to the irradiation. Furthermore, the measured signal attenuation and cross talk along the 7 cm long bus structures before and after the irradiation indicated no significant difference.

C. Full Scale Prototypes and Yield

The mentioned feed through connections from the sensor pad to a pad in the uppermost Cu layer, to be used for the bump connection to the FE chip, needs special care. Four vias are needed for each of these structures, i.e. for each pixel cell, to connect the cell's output pad to a component layer pad. As there are more than 61,000 interconnection structures with nearly 250,000 vias in a single module, a third test program has been set up with IZM to determine experimentally the via yield in MCM-D's and to study in addition the procedure of flip-chip assembly onto the MCM layers. Here four 2 μ m thick Cu layers interleaved with 5 μ m thick BCB layers have been deposited onto "dummy" sensor substrates. The vias in the uppermost BCB layer (component layer) are opened to allow for solder ball junctions to flip-chip assembled "dummy" FE chips. Full scale modules with 16 FE chips bump bonded to

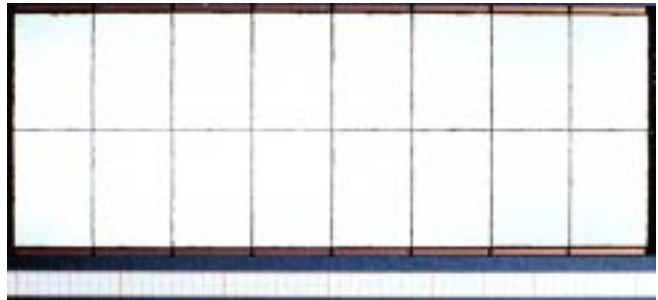


Figure 6: Photograph of a "dummy" module in MCM-D technology with 16 flip-chip assembled FE chips.

the substrate have been built. A photograph of one of these modules together with a mm scale is shown in Figure 6.

Figure 7 shows a cut through a module, illustrating the deposit of four 2 μ m thick copper layers separated by four 5 μ m thick Photo-BCB layers. The cut is placed through the solder balls which connect the upper metal layer to flip-chip assembled dummy read out chips. The via openings are 25 μ m in diameter. The figure in the left part shows the critical distance between the centers of two solder balls in adjacent pixel cells, a distance of only 50 μ m. The photo on the right shows the complete feed through connection from the substrate to the solder ball which is placed exactly above the substrate pad. From more than 1.1 million monitored vias a defect rate of less than 10^{-5} has been determined.

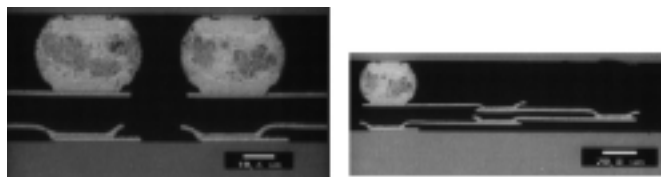


Figure 7: Cross section through the solder balls and the four metal and BCB layers of the MCM-D. (Photos Fraunhofer-IZM, Berlin)

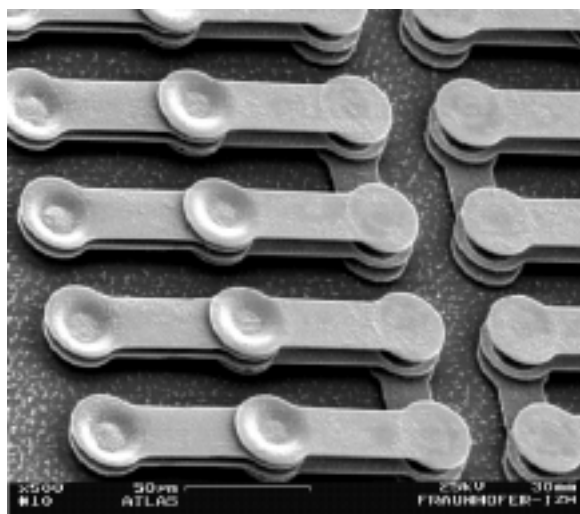


Figure 8: Cu structures from the substrate to the top metal layer, BCB etched for better visualisation. (Photo Fraunhofer-IZM, Berlin)

In the top view of Figure 8 one sees the (free standing) $2\ \mu\text{m}$ thick and $20\ \mu\text{m}$ wide feed through Cu structures from the substrate to the top metal layer. For a better visualization the BCB dielectric has been etched away. On the substrate one recognizes connections between pairs of two adjacent pads and no connection between two of such pairs. After the flip-chip assembly of dummy FE chips these "holes" are closed by appropriate connection paths within those chips. With such a set-up one builds a daisy chain for easy control of the quality of all interconnections including the bump connections. The results obtained in this phase confirm that an ATLAS type pixel module can be built using MCM-D technology and solder bump flip chip connections.

D. Demonstrator Module

As the *last step* before a module decision, a demonstrator module with a real sensor fabricated by CiS in Germany and by SEIKO in Japan assembled with real FE chips is being built by IZM. The design work of the signal- and power-bus below the end-of-column logic of the FE chips as well as the feed through structures within the active sensor area has been done and the mask production is completed. Measurements from this demonstrator module should give information on the passive components needed for the MCM-D type of modules. Due to the space available it is possible to place decoupling capacitors at the beginning and the end of the bus structures on both sides of the module. Because of the simple and not much disturbed electrical interconnection from the FE chip to the MCC this decoupling scheme might be sufficient. If it turns out that capacitors have to be foreseen for each FE chip then one has to enlarge the module (sensor/substrate) width by about 1.5 mm.

III. CONCLUSIONS

Due to the robust interconnection technology (only bump connections, no fragile wire bonds), and the encouraging results obtained so far, the MCM-D type module implementation appears to be a candidate building block for large area pixel detectors. On the interconnection bus signal lines separated by BCB dielectric layers from a reference plate result in controlled-impedance microstrip lines. This allows for fast signal transmission and low cross talk between adjacent lines. Two additional metal layers below the signal lines offer the possibility of low resistivity power distribution because of their larger widths. It has been demonstrated that the needed very high feed through density is achievable with present available MCM-D technology and that such a module can be built.

IV REFERENCES

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