Fabrication of a High-Density MCM-D for a Pixel Detector System using a BCB/Cu Technology

M. Töpper, L. Dietrich, G. Engelmann, S. Fehlberg, P. Gerlach*, J. Wolf, O. Ehrmann, K.-H. Becks*, H. Reichl

Technical University of Berlin

Fraunhofer Institute for Reliability and Microintegration Berlin, Germany

***Physics Department, University of Wuppertal, Germany**

Gustav Meyer Allee 25

D-13355 Berlin

phone: (+49)-(0)30-314-72845

fax: (+49)-(0)30-314-72835

e-mail: toepper@izm.fhg.de

Abstract

The MCM-D which is described here is a prototype for a pixel detector system for the planned Large Hadron Collider LHC at CERN, Geneva. The project is within the ATLAS experiment. A module consists of a sensor tile with an active area of 16.4mm x 60.4mm, 16 read out chips, each serving 24 x 160 pixel unit cells, a module controller chip, an optical transceiver and the local signal interconnection and power distribution busses. The extremely high wiring density which is necessary to interconnect the read-out chips was achieved using a thin film Copper/Photo-BCB process above the pixel array. The bumping of the read out chips was done using electroplating PbSn. All dies are then attached by flip-chip assembly to the sensor diodes and the local busses.. Focus of this paper is the detailed description of the technologies for the fabrication of this advanced MCM-D.

Key words: MCM-D, BCB, flip chip, pixel detector

Introduction

Large array pixel detectors are planned for the ATLAS project at the European Lab for particle physics in Geneva [1-3]. A modular system is needed which can be put together to build this large detector system. In general the diode-pixel-arrays (currently about 8 cm in length) and the read out chips (currently about 1 cm²) can be fabricated in wafer size dimensions. The highest packaging efficiency for this advanced electronic system is to use the concept of MCM-Ds in combination with flip-chip assembly. The silicon diode array is used as the substrate i.e. the basic building block for the detector system. The read out chips are then flip-chip bonded onto this module wiring the data lines, control lines, and power distributions to the periphery of the module. The module is working at frequencies in the range of 40 MHz. A microstrip line configuration will take care that line capacitances and line resistances do not cause RC-line charging which may slow down signal speeds quite considerably. A combination of a low k dielectric (BCB) with electroplated Copper is used to build-up this MCM-D multilayer. The interconnection between read out chips and sensor substrate is done by flip-chip technique using electroplated solder bumps. The advantage of this approach is to achieve highest integration density with best frequency behavior in a reliable process.

Design of the MCM-D

A module consists of a sensor tile with an active area of 16.4mm x 60.4mm, 16 read out ICs, each serving 24 x 160 pixel units, a module controller chip, an optical transceiver and the local signal interconnection and power distribution busses. Two pixel detector substrates were on each 4“ wafer. A four layer thin film metallization is necessary for routing the power, ground and signal layers. The signal lines were designed in microstrip line configuration. The signal layers are bus lines for the interconnection of the read-out chips. The link between the silicon pixel cells and the flip chip contact pads were realized using vias of staggered and staircase type. This was only achievable by an high-dense multilayer metallization. A maximum of 25 µm for the diameter of the vias were allowed by the design rules. On the other hand side a minimum of 3µm thick isolation between the metal layers was demanded. A photo polymer process was recommended because of the number of process steps i.e. cost. Photo-BCB was chosen because of matching physical parameters and the process technology of the polymer. 3 µm Copper was electroplated for the metallization. For Copper lines of width w =20µm, thickness t=2.2µm with a line spacing s = 30µm, a BCB dielectric thickness h = 8µm one computes for a microstrip line configuration a typical line capacitance of 1.2pF/cm with a time of flight of about 55 psec/cm. The characteristic impedance is around 50Ω and the voltage coupling to the neighbored line is estimated to be -20dB. For a 7cm long line the signal attenuation is about 30%.

Technology

Thin Film Multilayer

The thin film process was done using the 4“/6“ line @ Fraunhofer IZM / TU-Berlin. Polymers are preferred for the dielectrical layers in the MCM-D technology because their low dielectrical constant and the minimum loss tangens α allows thinner insulating layers and a higher pitch for the electrical wiring. Especially the IC industry is now confronted with the physical and processing limitations of inorganic interlayer dielectric (ILD) materials and is now introducing low k dielectrics in combination of Copper. In general the dielectric coating must be capable to the high-performance packaging technologies. Polyimides (PI) and Benzocyclobutene (BCB) are the only commercial available thin film polymers having a low dielectric constant and a high thermal stability. Using photosensitive polymers requires even fewer processing steps for multilayer wiring than dry-etching non-photosensitive materials. The advantage of Photo-BCB (Cyclotene™ , Trademark of The Dow Chemical Company) compared to Photo-PI is its low dielectrical constant and dielectric losses, minimal moisture uptake during and after processing and very good planarization. The BCB can be deposited by spin-coating directly over the Copper without any interdiffusion issues. The first established Photo-BCB process was based on the development system DS 2100™ [4,5]. A comprehensive overview is given in [6]. A batch development system which was used for this module was introduced for large area substrates, thick layers and high density, small vias [7,8]. BCB has a moderate curing temperature compared to PI which is important for the pixel detector substrate. A low electrical resistivity of the wiring system is achieved by electroplating Copper. A sputtered layer of Ti:W/Cu (100/200 nm) serves as a plating base. A positive working photoresist from Kalle-Hoechst is applied to create the plating mask. After metal deposition the plating base is removed by a combination of wet and dry etching. In figure 1 the thin film Copper/BCB process is summarized:

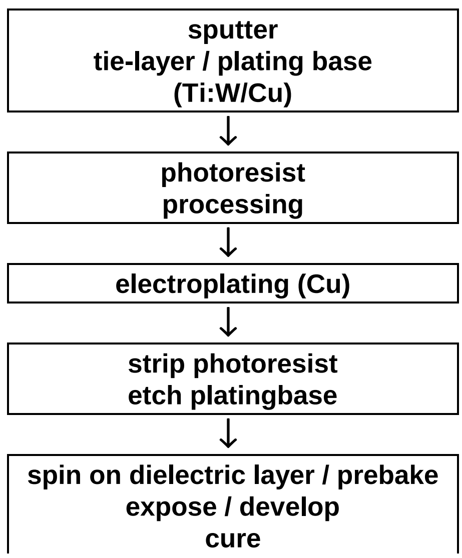

Figure 1: Thin Film Cu/BCB Process

Bumping

The pitch of the I/Os of the pixel detector is 50µm therefore PbSn bumps were plated for the flip chip assembly of the read-out chips. 16 chips were assembled on the multilayer detector substrate.

The detector wafers had Aluminium alloy pads with an inorganic passivation. The bumping process flow of Fraunhofer IZM / TU-Berlin is shown in figure 2.

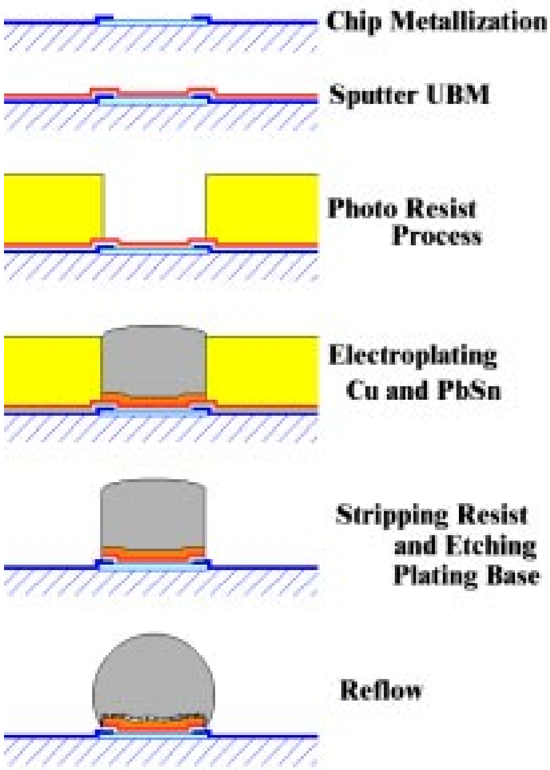

Figure 2: Process flow of Fraunhofer IZM / TU-Berlin for bumping by electroplating PbSn

The first step is the backsputtering of the Al using Ar to remove the Aluminiumoxide. A layer of 200nm Ti:W is then sputtered on the whole wafer as an adhesion layer and diffusion barrier, followed by a second layer of 300nm Copper which is used as the plating base. The titanium-tungsten has to protect the pad metallization against the formation of intermetallics of Al and has a high thermal stability, low electrical contact resistance and a very high adhesion to the Copper. The sputter condition are optimized to low stress deposition of the metals. High viscous photoresist is used to produce resist layers with a thickness of 5µm to up to nearly 50µm by one spin coating and patterning process [9]. For this high end application of the detector system a optimization of the photoresist process was necessary to achieve a yield of nearly 100%. Before the plating base is etched, the photoresist has to be removed without any residues. Essential for a wet etching process is that the etchant should erode the thin film plating base uniformly and completely but avoiding underetching. Underetching for Ti:W is below 1µm on 6" wafers using the process developed @ Fraunhofer IZM and TU-Belin.

The omic resistance of the electroplated PbSn bumps is approx. 2mΩ for 100x100µm bumps. Figures 3 and 4 shows the 25µm bumps with a pitch of 50µm before and after reflow.

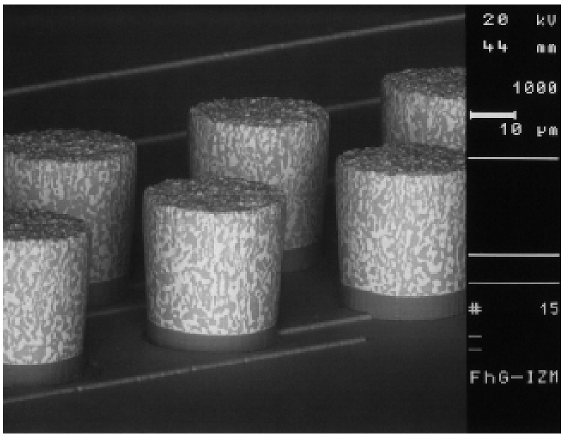

Figure 3: Eutectic PbSn bumps on 5µm Cu pedestal with a pitch of 50µm after etching the plating base (SEM)

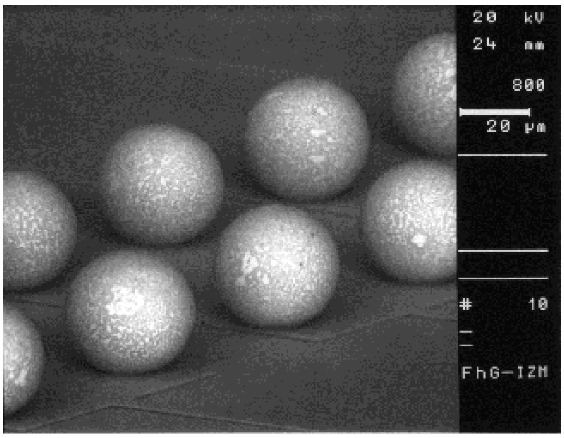

Figure 4: Plated PbSn of figure 3 after reflow (SEM)

Results

The pictures 5 to 7 show parts of the multilayer Copper/BCB wiring system. As BCB is transparent one can see the different types of feed-through elements (staggered and staircase type).

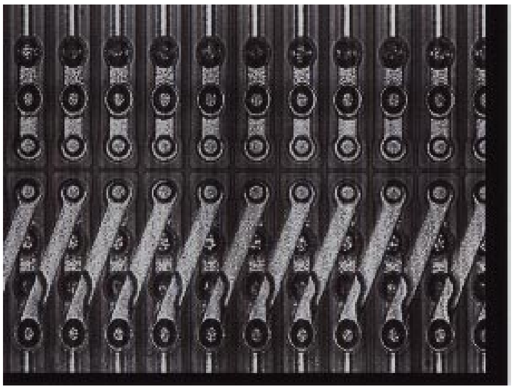

Figure 5: Top view of one of the 4 metal feed through configuration (video print)

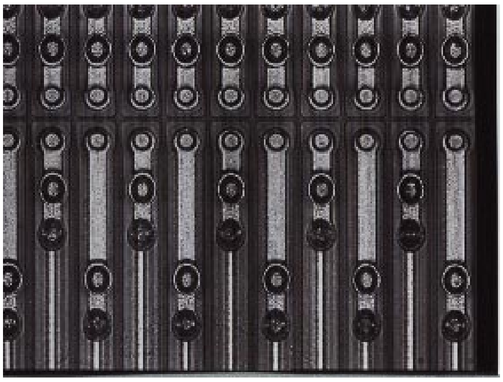

Figure 6: Top view of one of the 4 metal feed through configuration (video print)

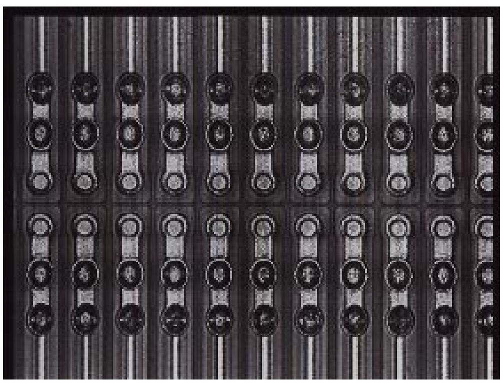

Figure 7: Top view of one of the 4 metal feed through configuration(video print)

Figure 8 shows a via in the Photo-BCB with a diameter of 25µm mask dimension.

Figure 8: Top view of a via in the Photo-BCB with a diameter of 25µm mask dimension (video print)

Test structures for the evaluation of the electrical resistivity of the vias were measured. Vias chains with vias down to 10µm diameter (mask dimensions) are possible as shown in figure 9.

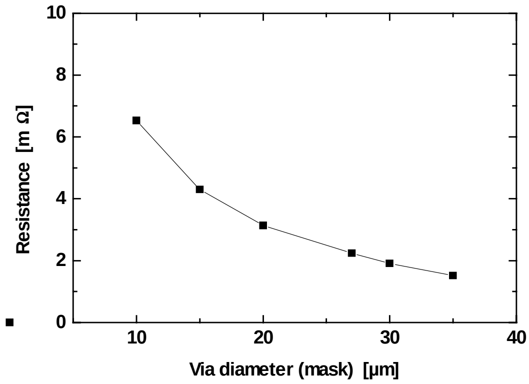

Figure 9: Via resistance vs. via diameter (mask dimensions)

The electrical resistance of each via designed for this pixel detector module is around 5mΩ per via. This gives 60 - 160 mΩ per feed through element.

The results show that it is possible to build highest density MCM-Ds with more than 6000 I/Os per cm^2 through a multilayer BCB/Cu Si-substrate. Four via layers are needed for the feed through connections from the sensor pad to a pad in the uppermost Cu layer, to be used for the bump connection to the read out chips. As there are more than 61,000 interconnection structures with nearly 250,000 vias in a single module, a test program has been set up to determine experimentally the via yield of the thin film multilayer and to study in addition the procedure of flip-chip assembly onto the MCM layers. Here four 2 µm thick Cu layers separated by 5 µm thick Photo-BCB layers have been deposited onto "dummy" sensor substrates. The vias in the uppermost BCB layer (component layer) are opened to allow the solder joining of the read out chips. Full scale modules with 16 read-out chips bump bonded to the substrate have been built. From more than 1.1. million monitored vias a defect rate of less than 10^{-5} has been monitored. In figure 10 the 2µm thick and 20µm wide feed-through elements are shown For better visualization in the SEM the BCB was etched by RIE.

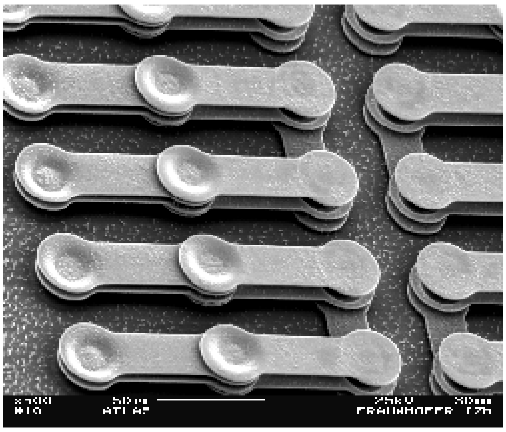

Figure 10: Cu feed through elements from the substrate to the top flip-chip interconnection layer (BCB was etched by RIE for better visualization) (SEM)

The connections between pairs of the feed through elements are shown on the substrates which are connected by the flip chip assembled devices as shown in figures 11 and 12.

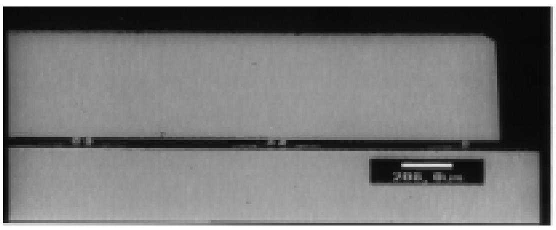

Figure 11: Assembled Flip Chip device (cross section

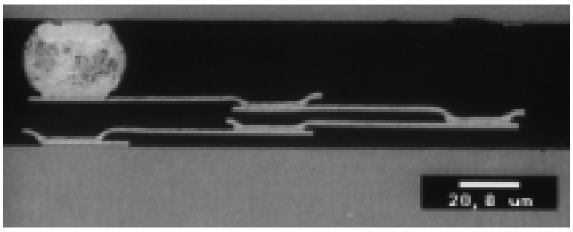

Figure 12: Cross section through the solder balls and the four layer metallization (Cu/BCB)

Figure 13 shows part of the detector substrate with the 4 layer Cu/BCB metallization. Thin high-density signal lines are close to the wide power planes which is challenge for the Copper/BCB process.

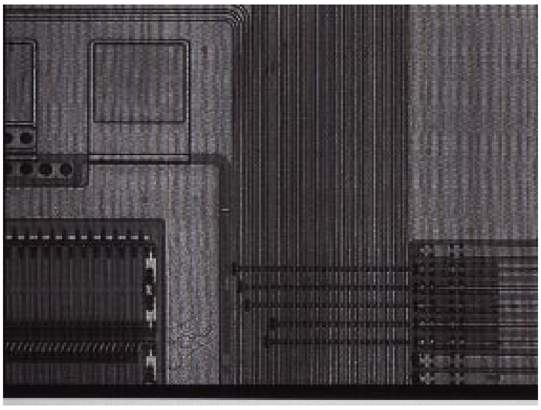

Figure 13: Photograph of the detector substrate with the 4 layer Cu/BCB metallization

Figure 14 shows the demonstrator module with the sensor chips fabricated by CiS (Germany) and Seiko (Japan). The packaging density allows additional passive components to be assembled which will be evaluated in the future.

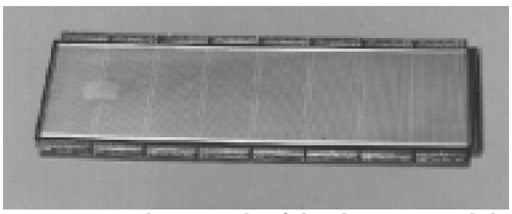

Figure 14: Photograph of the detector module with 16 flip chip bonded read-out chips

As the detector elements are located very near to the circulation beams the MCM-D has to be radiation tolerant enough to survive the expected life time. The degradation of the

BCB due to the irradiation has been examined by analyzing the effective relative permittivity because the detector elements are located near the circulating beams. Only changes in the range of 1.5 to 2.5% could be measured.

Reliability

Thermal cycling (-65°C / +155°C, 10 min dwell, 20 min ramp) of a two layer Cu-Photo-BCB-Cu teststructure (via-chains) was done. 2000 cycles were passed without any degradation in the electrical resistivity of the vias. The same test-structures passed also 2000 hours at 85 % humidity and 85°C.

During thermal aging @ 150°C the contact resistance of the PbSn bumps hardly changed, as only a slight increase of 0.2 mΩ was observed after 1500 hours [10]. The reliability of the bump metallurgies under operation conditions was checked by MIL-STD-883 (AATC -55°C to +125°C). At a shear height of 8µm, which is well above the Copper-tin intermetallics, always ball shear was observed without any delamination. Over 4000 cycles were passed without any significant change in the shear force.

Conclusion

It was demonstrated that this MCM-D approach is an excellent combination of high integration density, very good frequency behavior and high reliability for this pixel detector system. Two Copper layers separated by the low k BCB allow for fast signal transmission and low cross talk between adjacent signal lines on the interconnection bus lines. The microstrip lines result in controlled impedance transmission signal lines. It was demonstrated by TUB / Fraunhofer IZM that the defect rate of such a high density four layer metallization was only 8.13 e-6 . Only 9 vias of 1.2 millions were not open. This MCM-D type module in combination with flip chip technique is therefore a promising candidate as a building block for the large area pixel detector because it combines high reliability with highest packaging density both most important for this high-end application.

Acknowledgment

The authors wish to thank Ch. Kallmayer, C. Meinherz, C. Karduck and E. Busse for their technological support.

Literature

[1] K.-H. Becks et al. „A Multi-Chip Module, the Basic Building Block for Large Area Pixel Detectors“ Proceedings of IEEE MCM Conf. (19996) 16

[2] J. Wolf, P. Gerlach, E. Beyne, M. Töpper, L.Dietrich, K.H. Becks, N. Wermes, O. Ehrmann, H.Reichl „High Density Pixel Detector Module using Flip Chip and Thin Film Technology“ proceedings ISPS 1999

[3] K.H. Becks, E. Beyne, O. Ehrmann, P. Gerlach, I. Gregor, P.Pieters, M. Töpper, C. Truzzi, J. Wolf „A MCM-D-type Module for the ATLAS Pixel Detector“ IEEE Nucl. Science Symp. 1998, Toronto

[4] G. Chmiel, M. Töpper, Ch. Jöhren, A. Achen „Thinfilm MCMs, Process Development using Photosensitive BCB“ Proceedings of Microsystem Technologies `94, Berlin Oct 1994, Berlin.

[5] M. Töpper, J. Wolf, V. Glaw, K. Buschick, A. Dabek, L. Dietrich, O. Ehrmann, H. Reichl „MCM-D with Embedded Active and Passive Components“ Proceedings ISHM Conference, Minneapolis, 1996

[6] A.J.G. Strandjord, Y. Ida, P.E. Garrou, W.B. Rogers, S.L. Cummings, S.R. Kisting“ MCM-D Fabrication with Photosensitive BCB: Processing, Solder Bumping, System Assembly and Testing“ Proceedings of ISHM 97, Los Angeles Oct. 1995.

[7] M. Töpper, K. Scherpinski, R. Hahn, O. Ehrmann, Ch. Schmaus, F. Bechthold, H. Reichl „ Combination of MCM-C Technology with MCM-D Technology using Photosensitive Polymers“ roceedings of the 4th Internat. Sympos. on Advanced Packaging Materials, Braselton (USA), Mar. 15-18., 1998

[8] M. Töpper, M. Schaldach, S. Fehlberg, C. Karduck, C. Meinherz, K. Heinricht, V. Bader, L. Hoster, P. Coskina, A. Kloeser, O. Ehrmann, H. Reichl „Chip Size Package - The Option of Choice for Miniaturized Medical Devices - Proceedings IMAPS Conference San Diego 1998

[9] D. Tönnies, M. Töpper, J. Wolf, G. Engelmann, H. Reichl „ Mask Aligners in Advanced Packaging“ Solid State Technoogy, March 1998

[10] L. Dietrich, J. Wolf, O. Ehrmann, H. reichl „Wafer Bumping technique using Electrolplating for High-Dense Chip Packaging“ 3rd Intern. Symp. on Elecrtronic Packaging Tech., Beijing, Aug. 1998.