

The Control System for the ATLAS Pixeldetector

M. Imhäuser, K. H. Becks, S. Kersten, P. Kind, P. Mättig, and J. Schultes

Abstract—For the ATLAS experiment at the LHC (Large Hadron Collider), CERN, a pixeldetector is under construction. Due to the large number of channels a data-intensive control system will be required. The choice and design of its hardware is mainly driven by the high power density and the harsh radiation environment. This includes the development of an interlock system, which is responsible for the safety of the detector, and a special control and supply system for the operation of the optical link. To account for the complexity of the system a commercial SCADA (supervisory control and data acquisition) system is used. Based on this we developed a geographical approach, which combines the different hardware components for one detector part to uniform software elements. Its tree structure allows a clear control of the large number of information. For the realization a distributed system, where several SCADA systems are linked, is necessary. We have shown this system to work efficiently and will discuss first experiences.

I. INTRODUCTION

The pixeldetector is the component of the ATLAS inner tracker closest to the interaction point. Its central part is built up by three shells, the support structures for the staves, to which the detector modules themselves are attached. In the endcaps three disks each are carrying the modules. This gives in total 1744 detector modules. From the DCS point of view a module is the smallest unit to act on. It consists of a silicon sensor with a ‘pixelated’ structure and 16 frontend readout chips. A flexible hybrid circuit, glued to the top of the module, carries the Module Controller Chip, which organizes the data transmission from the module via a bi-directional optical link.

The pixeldetector control system can be divided into two parts: the frontend and the backend system. The former consists of sensors (e.g. for measuring temperatures), readout units like ADCs and the microcontrollers, which handle the data transfer to the backend system. This is the higher level software, which is responsible for data storage, the link to the ATLAS wide control system and the communication to the data acquisition system. It also has to supply the user with graphical interfaces.

II. THE FRONTEND SYSTEM

As can be seen in Fig. 1, the frontend system of the pixeldetector is built by various hardware components of different functionality. About 450 frontend nodes are sending their information to the local control station, while one node controls up to 150 channels. (The numbers in Fig. 1 are still preliminary, as e.g. the modularity of the low voltage system might change, see below.) The main components of the frontend system will be described in the following sections.

A. The Power Supplies

Various voltages are necessary for the operation of the detector. Two low voltages supply the readout electronics, the high voltage is used for the depletion of the sensors. Additionally three low voltages and a control signal are used for the operation of the optical link, see below. In order to support the ATLAS grounding scheme, all voltages must be floating.

For the two former a commercial solution is aimed for. The systems should have a high level of local intelligence, which enables them to operate autonomously. A system, which is not relying on the functionality of the network, reduces the network traffic and - as it is able to react to error conditions by its own - enhances the safety of the detector.

The modularity, how many detector modules are connected to one power supply channel, is still under investigation. A good compromise between costs and redundancy must be found.

Due to the sensitivity of the readout chips to transients, regulators are necessary in the related power supply lines. As the location should be as close as possible to the detector, radiation hardness is the demanding requirement to these regulators.

Therefore the L4913, a device developed by ST Microelectronics, Italy, in the framework of the RD 49 project at CERN is chosen. Regulator units, a monitor and control system using FPGAs and the ELMB are presently under development [1].

B. The Cooling System

The high power density of the on-detector readout electronics requires an efficient cooling. Therefore a system based on the evaporation of per-fluoro-n-propane (C3F8) is chosen [2]. Advantages of this refrigerant are that it is non-

flammable, non-conductive and radiation resistant, and that it helps to reduce the material inside the tracker's sensitive volume (flow rates 1/20 of those in a mono-phase liquid system). In total about 15 kW of heat are removed by 80 'parallel cooling circuits' (PCC).

A separate control system, specially adapted to the requirements of regulation circuits, will be used. The status information of the PCCs will be sent to the local control station and included there in the overall detector control system.

C. The ELMB

The Embedded Local Monitor Board (ELMB), developed by the ATLAS DCS group, is a multi purpose, low cost, data acquisition and control device [3]. The local intelligence of the ELMB is provided by the ATmega128L, a microcontroller manufactured by ATMEL. The main monitoring and control applications run on this processor. 64 16-bit, multiplexed ADC- and 34 digital I/O-channels are available. Further devices, like a DAC, can be controlled using the SPI-bus. The communication with the local control station is realized with the CAN fieldbus using the CANopen protocol.

In the pixel detector control system the ELMB is used for various monitoring and control purposes, all together on about 190 devices. Based on the ELMB two detector specific applications are developed: the thermal interlock and the so called SC-Olink system.

D. The Thermal Interlock System

As the operation temperature of the detector determines its longevity, each detector module is equipped with a temperature sensor. This sensor should be very robust and must be able to stand the harsh radiation environment ($2 \cdot 10^{15}$ n/cm² in 10 years operation of ATLAS). Therefore a thermistor was chosen. Its signal is fed to an ADC for monitoring. In parallel it is led to the input of an interlock box, which generates in case of heat ups a signal acting on the related power supply channel, see Fig. 2. This protects the detector against failures in a cooling circuit or de-lamination of a single detector module from the cooling structure. As individual power supplies can be switched off, the number of modules out of operation can be minimized.

To reduce the influence of noise and to avoid a four wire measurement, a 10 k Ω NTC from Semitec, Japan, the 103KT1608-1P type, was chosen. The relative changes of its resistance of 4 % per Kelvin and a 1 % precision at 25 °C are fitting our requirements. Another advantage is the radiation hardness of its glass coating.

In the electrical circuit of the interlock box any multiplexing or initializing via software is avoided. Therefore a completely independent operation is possible. On the other hand the design has to be compatible to the ELMB. A reference voltage is delivered by the reference section and supplies the NTC via a precision resistor. The signal from the sensor is compared to different thresholds. The following

nor-gates generate a 2-bit pattern. The four different states indicate: okay, temperature too high, temperature too low, broken cable.

As the location of the interlock box will be in the ATLAS cavern, all components must be radiation tolerant. We aimed to use standard devices, therefore intensive irradiation studies were performed, to find a set of components to stand the radiation levels defined by [4]. The final set of components can be found in [5]. Using these devices the interlock box is able to tolerate 100 Gy and $5 \cdot 10^{11}$ n/cm² (1 MeV), which correspond to a 10 year operation inside the ATLAS cavern.

The thermal interlock system is completed by the 'logic unit'. To account for different modularities in the power supply scheme, it can combine interlock signals from several detectors modules and split the signal on the power supply channels. As the location of the logic unit will be in a radiation free area, the choice of components is not that critical.

Several studies, including system tests with original cable length (150 m), have shown that the thermal interlock system works very reliable. Without individual calibration of the channels the expected error for the overall chain of ≤ 0.5 K can be met.

This thermal interlock system is also foreseen for the protection of the regulators and the 'opto' boards, see below. Another usage of the interlock box will be the control of the heaters on the 'thermal barriers'. In this case the temperature low signal will be used to power the heaters if the temperature falls below the dew point.

E. The SC-Olink System

An optical data transfer will be used for the connection between detector and read out crate. Each link consists of two transceiver diodes and two control chips, seven links are located on one 'opto' board. For its operation 4 different channels are required: the supply voltage for the control chips, the depletion voltage for the receiver diode, a current to control the transmitter diode and a reset signal. These channels build the Support and Control – Optolink System (SC-Olink System). Again floating outputs is a demand. As the power consumption of three of these channels is quite low, a solution based on DC/DC converters and a DAC followed by a power amplifier seems feasible, see Fig. 3. Using the SPI-bus, the DAC can be controlled via the ELMB. Its internal software [6] already supports this approach.

Such a system is under development. First circuits were operated successfully. With the 12-bit DAC from Maxim (MAX5122) a precision of better than 0.5 % was achieved, while the maximum output power being 20 V and 20 mA. The ripple of 10 mVpp seems to be low enough for our requirements. Additionally a hardware current limitation is foreseen. The electrical diagram can be found on [7].

F. The OPC Server

The link between the low level software running in the microcontrollers of the frontend system and the higher level software running on the local control station is realized via OPC (OLE for process control). This is an open and manufacturer independent standard. It is based on the idea that each type of hardware device has its own OPC server to which diverse applications (the OPC clients) can connect to. The communication between server and client is not limited to one local computer and can also take place via TCP/IP. Three OPC servers were successfully used till now: the CAEN OPC server 1.1, the CANopen OPC server 2.5 and the ISEG OPC server 1.14.

III. BACKEND SYSTEM

The core of the backend system, the higher level software running on the local control station(s), is a SCADA system. Following the LHC wide recommendation a commercial solution is chosen here: PVSS (Prozess, Visualisierungs- und SteuerungsSystem, by ETM, Austria), [8].

A. PVSS

PVSS supplies a set of tools to build a control system. It runs under Windows and Linux operation systems, offers graphical user interfaces (GUI) and supports 'distributed' systems for the construction of large systems, (see chapter III.C).

PVSS is designed as a system where special tasks are fulfilled by separate 'managers'. The communication between them follows the client-server model. Using separate managers offers the advantages that the processes can be scattered on different processors or that different priorities can be assigned to the individual managers. The main process is the event-manager, which interacts between the driver-, control-, database-managers and the graphical user interface.

Devices are represented via datapoints (DP), whose structure is given by the datapoint-types (DP-type). Within the DP-type the structure is defined by DP-elements, leaves and nodes. While a leaf contains the physical data and their configuration, a node can consist of further nodes and leaves. In this way a tree structure is built. In addition it is possible that a node inherits the structure of another DP-type. This device oriented concept allows a flexible and hierarchical mapping of components onto the system.

B. FIT

As the ELMB will be used in several applications of the pixel-DCS, a concept based on the principles described above was developed for the integration of a large number of equal devices: the 'Frontend Integration Tool' (FIT). For each component a DP-type was defined. Via control scripts the desired number of DP can be created and configured. In order to keep this flexible, the choice of these global constants is accessible via a GUI. The consistency of the entries is checked immediately and the corresponding OPC

configuration file for the communication to the hardware is created.

In this way FIT was used to determine the actual configuration of the CAN, to choose the number of ELMBs currently connected and to select the ADC operation parameters. Also calibrations can easily be executed.

As FIT turned out to be very sufficient and user friendly it was already used for the preparation of various setups and we also started to use this concept for the integration of other devices into PVSS.

C. Distributed Systems

During tests with constituents of the control system it turned out that just one local control station will be insufficient to handle the data volume of the final system. Therefore we enlarged the system using a distributed system, which is composed of two or more standalone PVSS systems, each having its own event and data manager [9].

To investigate the performance of such a system, we installed a setup of four PVSS systems with different readout chains. The used PCs differed in speed and memory size. Three stations were responsible for data taking and processing, while the fourth was the 'master station'. With the data received from the subsystems, a GUI running on the master station was able to inform the user about the actual status of the whole system, (see Fig. 4).

Under normal conditions the system was running stable. However during start up delays were observed. A clear dependence of the used PC, its speed and memory size, could be seen. Nevertheless all data were processed without errors and stored with correct time stamps.

The restriction of the actual PVSS version (2.12.1), that all required DP-types must be defined identically on all systems including their internal identification number, should be fixed by the next version. Reliability issues, like broken connections, starting and stopping subsystems, network load and DB corruptions will be investigated then.

D. The Geographical Approach

To arrange the large number of channels in a clear way for the users who are not that familiar with the details of the control system we developed a geographical approach, (see Fig. 5).

This concept subdivides the status of the entire detector in the combination of states of smaller and smaller parts. In this way an inverse tree structure is built. In a first step the subdivision follows the partitioning of the data acquisition system (DAQ) imaging the distributed system. The next hierarchy is given by the independent circuits of the cooling system. The half staves (HS) or disk sectors (DS) respectively define the lowest level, the so called 'base detector unit' (BDU). Each BDU contains all information about the detector modules belonging to it, e.g. the depletion voltages, temperatures, functionality of the optical link etc. This helps shifters in understanding the operation of the detector and

specially makes - as all relevant information of a detector element is made available - error tracing easier.

If one BDU is defined, large parts of the detector can easily be composed by it, making use of the PVSS internal data structures, as described above. Adding further information to the BDU is also inherited automatically to all instantiations. For the final system it is aimed to implement a 'finite state machine' based on the geographical approach.

E. DDC

Proposed by the ATLAS control group the software tool 'DAQ-DCS communication (DDC)' is chosen for the connection between the DAQ (data acquisition) and the pixeldetector control system. The interface point for the DAQ side is the online software while DCS uses the 'application programming interface' of PVSS to connect the DDC [10]. The software package includes three components of communication which operate completely independent of each other: ddc_dt transfers data like temperature of a pixel module or the DAQ run state in the corresponding direction; ddc_ct sends DAQ commands like 'prepare for run' to DCS and returns the response; ddc_mt delivers DCS messages like alarms to DAQ. To configure the DDC the usage of the TDAQ configuration database is under investigation. Further we study which data, commands and messages are necessary for the operation of the pixeldetector.

IV. SUMMARY

The safety requirements of the ATLAS pixel detector have made specific developments necessary for the hardware components of the DCS (detector control system). A thermal interlock system, which - in case of heat ups of single detector modules - switches off the associated power supplies, is developed. Its main characteristics are a radiation tolerance of 5 E11 n/cm² and 100 Gy and an accuracy below 0.5 K for the whole circuit.

For the operation of the optical link a supply and control system is under development. Its design is based on the ELMB controlling a DAC. First prototypes showed a precision of better than 0.5 % and a ripple below 10 mVpp.

The core of the software is built with the commercial product PVSS. For integration of the hardware devices into PVSS a special tool, FIT, is developed. Using it, a flexible configuration and operation of the CAN fieldbus and its related ELMBs is possible.

To describe the mapping between the hardware channels and its presentation in the software including the user interfaces, we used a 'geographical approach' which defines a hierarchical structure. The pixeldetector is composed of several layers, the lowest one given by the so called base detector unit, which contains all physical information (like temperatures, voltages, etc.) for a single detector element. While setting up a first control system, it has been shown that our concept is well supported by PVSS' data structure.

Because of the large number of channels to be monitored and controlled, a so called 'distributed system' will be

required, which enables to split the whole control system onto several, interconnected computers. Every computer with its own PVSS system is responsible for the control of one detector part. The additional master station makes the connection to the outer world.

With the distributed system the technical basis for the control system of the pixel detector is created. The representation of the data is described by our geographical approach. Due that our control system is now - by adding more and more BDUs - easily expandable towards the final system. With this system further questions like the communication to the data acquisition system and the data-transfer to the conditions-database can be studied.

V. REFERENCES

- [1] M. Citterio INFN Milano, private communication
- [2] E. Anderssen et al, "Fluorocarbon Evaporative Cooling Developments for the ATLAS Pixel and Semiconductor Tracking Detectors", Proc. 5th Workshop on Electronics for LHC Experiments, CERN 99-09 CERN/LHCC/99-33
- [3] <http://atlas.web.cern.ch/Atlas/GROUPS/DAQTRIG/DCS/ELMB/elmb128.html>
- [4] M. Dentan, "ATLAS Policy on Radiation tolerant Electronics", ATC-TE-QA-001
- [5] S. Kersten, P. Kind, "Technical Description of the Interlock Circuit and System of the ATLAS Pixel detector" ATL-IP-ES-0041
- [6] <http://www.nikhef.nl/pub/departments/ct/po/html/ELMB/ELMBresources.html>
- [7] <http://www.atlas.uni-wuppertal.de/dcs>
- [8] <http://www.pvss.com>
- [9] P. Burkimsher, "Scaling up PVSS, Synthesized Requirements" <http://cern.ch/itcobe/Projects/ScallingUpPVSS/Documents/synthesizedRequirements.pdf>
- [10] V. Khomoutnikov, "ATLAS DAQ-DCS Communication Software, User's Guide", http://atlasinfo.cern.ch/ATLAS/GROUPS/DAQTRIG/DCS/DDC/ddc_urd.ps

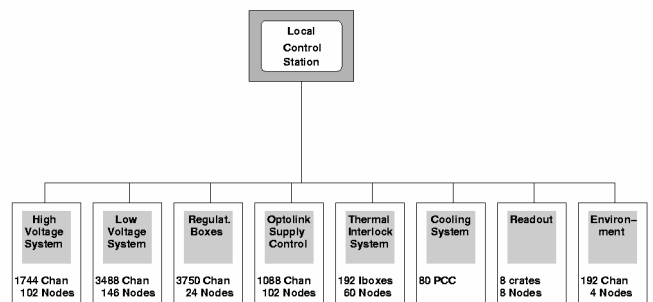


Fig. 1. Functional Blocks of the Pixeldetector Control System

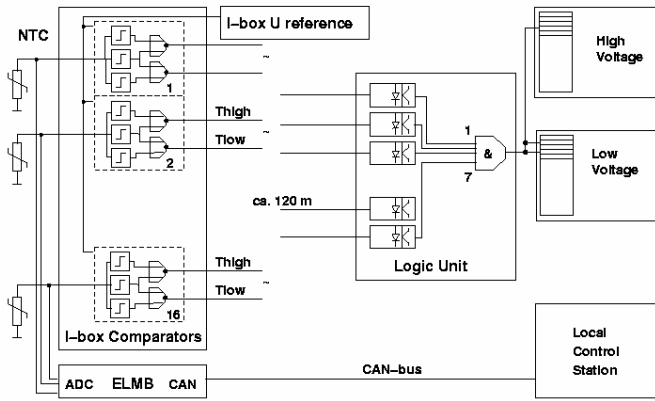


Fig. 2. Schematic of the Thermal Interlock System

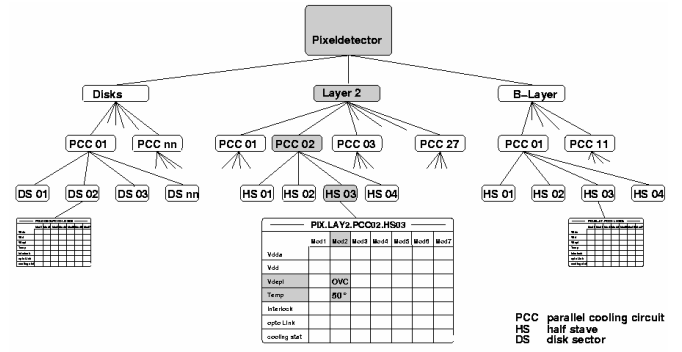


Fig. 5. The geographical Approach

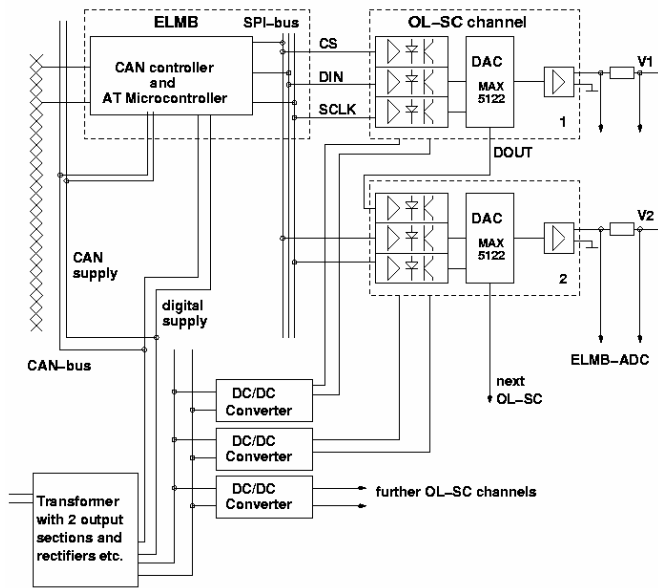


Fig. 3. Schematic of the SC-Olink System

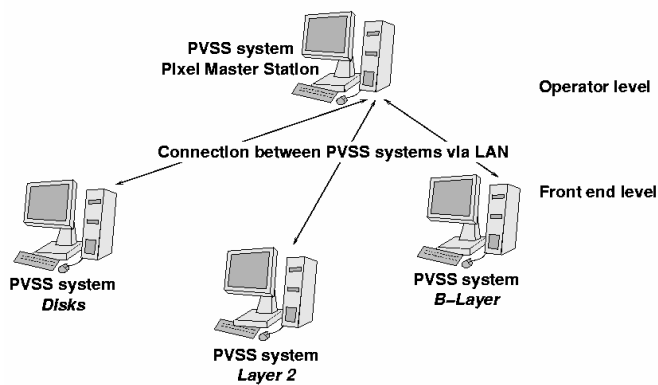


Fig. 4. Distributed Systems