

The hardware of the ATLAS Pixel Detector Control System

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ABSTRACT: The innermost part of the ATLAS (A Toroidal LHC ApparatuS) experiment, which is currently under construction at the LHC (Large Hadron Collider), will be a silicon pixel detector comprised of 1744 individual detector modules. To operate these modules, the readout electronics, and other detector components, a complex power supply and control system is necessary. The specific powering and control requirements, as well as the custom made components of our power supply and control systems, are described. These include remotely programmable regulator stations, the power supply system for the optical transceivers, several monitoring units, and the Interlock System. In total, this comprises the Pixel Detector Control System (DCS).

KEYWORDS: Particle tracking detectors; Detector control systems (detector and experiment monitoring and slow-control systems, architecture, hardware, algorithms, databases); Voltage distributions.

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1. Introduction

The pixel detector is the sub-detector located nearest to the interaction point, and has the main goal to reconstruct secondary vertices, such as those present in the decays of B mesons.

In order to obtain the necessary resolution for this task, the pixel modules have individual pixels of dimensions $50\ \mu\text{m} \times 400\ \mu\text{m}$, with a total of 46080 pixels per module. In the barrel part of the detector, the modules are loaded onto linear mechanical supports referred to as staves, which are then mounted onto three concentric shells. In the end caps, the modules are mounted on sectors which are formed into disks, with three disks per end cap. The relevant granularity for the power and controls systems is the half-stave or disk sector, which is comprised of either six or seven modules, although some functionality at the single module level is also present.

A pixel module consists of the sensor which is bump bonded to 16 custom designed readout chips, with the readout chips having both analogue and digital circuitry. All communication for a module is handled by the module controller chip (MCC), which is mounted on a flex hybrid circuit affixed to the top of the module. Data transfer is handled by optical links, with the optoboard – the on-detector electro-optical transceiver – sending the data

over optical fibres to the back of crate (BOC) cards, which are located approximately 100 meters away in the counting rooms.

2. DCS hardware requirements

In addition to the functional requirements of the power supplies and monitoring units, there are some additional considerations which must be kept in mind. Specifically, the high power density inside the detector volume, as well as the radiation tolerance of components placed near the interaction point, affected the design of many components. Given that some elements will be inaccessible for long periods of time, reliability becomes even more important.

Furthermore, the design of the system has been driven by the need to find a good compromise between the desire to control and tune individual elements of the detector and a low cost.

The power supplies and all associated monitoring units must conform to the ATLAS grounding scheme, which requires a floating ground. Due to the effects of radiation on the pixel modules over a period of approximately ten years, all power supplies must have adjustable outputs. And for safety, all power supplies are required to have over-current protection as well as interlock inputs.

As all hardware must be integrated into the pixel and ATLAS DCS (Detector Control System), the interfaces of the various components must be compatible with them. Therefore, the ELMB (Embedded Local Monitor Board) comprises the core of all our applications [1]. The ELMB is a multipurpose acquisition and control unit, which possesses a CAN (Control Area Network) interface. Its communication is based on the CAN-open protocol, which was chosen by ATLAS DCS for its reliability.

3. Overview of the DCS hardware system

The DCS hardware system consists of (see figure 1):

- the power supplies needed to operate the detector modules and the optoboards
- the regulator stations
- temperature, humidity, and current sensors
- monitoring devices for the readout of the sensors
- the Interlock System
- the DCS PCs communicating with the hardware

Figure 1 provides a schematic overview of the DCS hardware, as well as a simplified representation of the Interlock System.

The pixel power supply system consists of four major components [2].

1. Two separate voltages are required to operate the front end electronics, Vdd (digital) and Vdda (analogue). These voltages are provided by commercial power supplies (PL512) from W.IE.NE.R (Burscheid, Germany), and are regulated by the Regulator Stations, which are located near to the detector.
2. The high voltage (up to 700 V and 4 mA) which depletes the detector modules is provided by the EHQ-F007n-F supply built by *iseg* (Rossendorf, Germany). As the high voltage does not require any further regulation, it is sent directly to the detector elements.

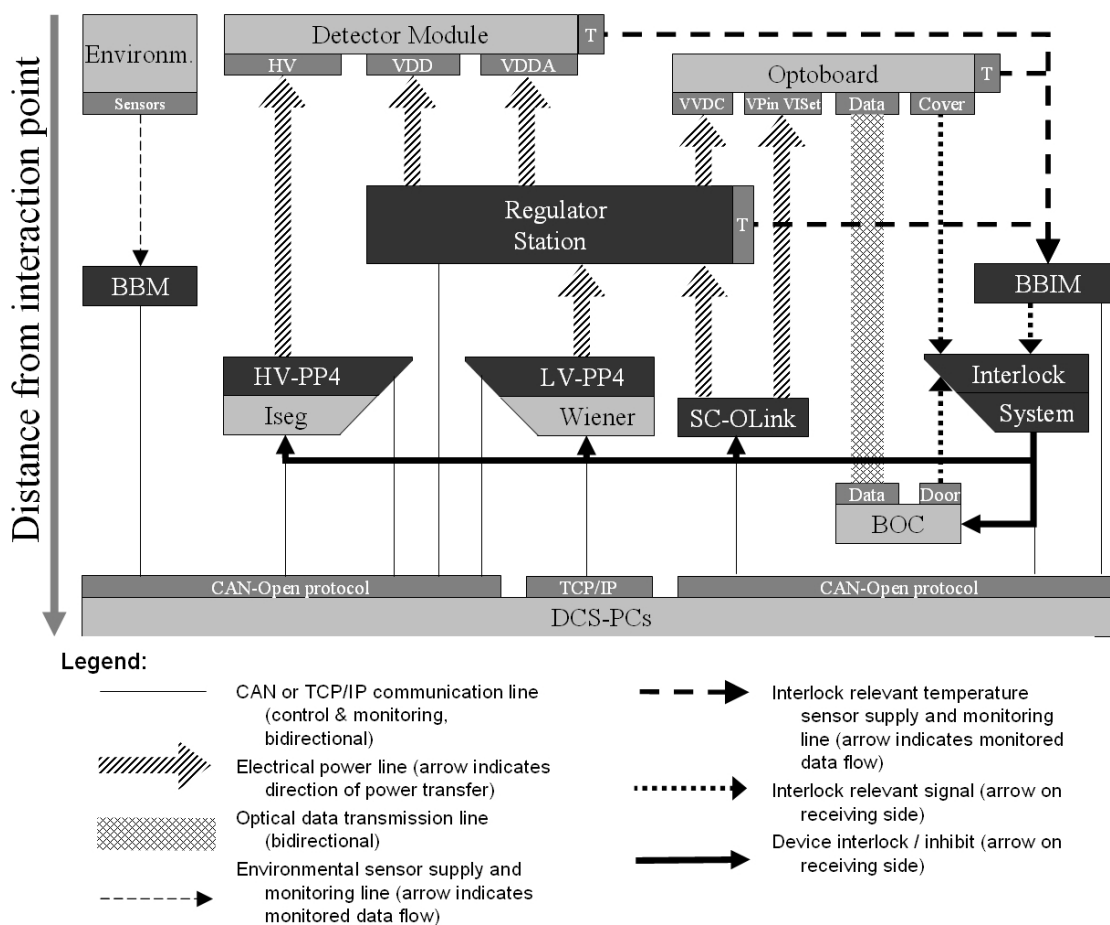


Figure 1. Overview of the DCS hardware (Interlock System simplified).

3. The related LV-PP4 (low voltage patch panel 4) and HV-PP4 (high voltage patch panel 4) units distribute the voltages and monitor the current consumptions for Vdd, Vdda, and the high voltage.
4. The optoboard voltages are supplied by the SC-OLink (Supply and Control for the Opto-Link).

Monitoring of various temperature and humidity values is performed by the BBM (Building Block Monitoring) and BBIM (Building Block Interlock and Monitoring) crates. While the BBM only provides for reading of values, the BBIM also creates logical signals which are fed into the Interlock System.

All of the main power supplies mentioned above (LV, HV, SC-OLink) plus the off-detector part of the optical link, the BOC card, are connected to the hardware-based Interlock System. This consists of several units that guarantee safety for human operators as well as for sensitive detector parts.

All primary power supplies, the Regulator Stations, the monitoring crates, and the Interlock System are connected to the DCS PCs via the CAN-Open protocol, with the exception of the low voltage crates, which are connected via TCP/IP.

4. Power supplies

All power supplies are located in the counting rooms, providing for easy access and flexibility during operation. In addition, this eliminates the need to consider the effects of radiation on their performance. However, it is desirable to have voltage regulation as near to the detector as possible, and not at this distance of more than 100 meters from the detector. This functionality is provided by the remotely programmable Regulator Stations, which protect the module readout chips against transients. They also provide the ability to individually tune and optimize the operational voltages for each detector module.

The low voltage and high voltage power supplies provide channels at the granularity of half-staves and disk sectors. The PP4 units then split these channels to provide individual supplies to each detector module. In addition, the PP4 crates provide current monitoring for single detector modules. This offers a good compromise between the costs of hundreds of power supply channels and the need for all available information pertaining to the detector modules.

The high voltage and low voltage power supplies are commercial systems, while the Regulator Stations and the SC-OLink are custom made.

4.1 Supply and control of the optical link

Three different voltages and one control signal are required to operate one optoboard. These four outputs comprise one SC-OLink channel [3]. The transceiver chips and the VCSEL (Vertical Cavity Surface Emitting Laser) components are supplied by V_{dc} (10 V, 800 mA), while the receiver diode is supplied by V_{pin} (20 V, 20 mA). The operating point of the VCSELs can be adjusted by varying V_{iset} (5 V, 20 mA), while the fourth output (2.5 V, 10 μ s) provides a reset signal to the receiver control chip. There are in total 272 of these SC-OLink channels.

The output voltages can be adjusted by means of a single channel DAC (MAX5122, 12 bit), which is controlled by an ELMB. Isolation of the floating outputs is ensured by transformers and optocouplers on all control and monitoring lines. As the DACs are powered separately, the output voltages remain unaffected if a power cycle of the CAN bus is necessary for resetting the ELMBs. The precision for both setting and monitoring is better than 0.5%. In addition, all channels possess a hardware current limitation, and there is one interlock input per channel.

4.2 Regulator station

To protect the integrated circuits of the front end chips against voltages surges or spikes, a remotely programmable Regulation Station capable of providing individual floating power output with low ripple has been designed. One Regulation Station can power up to 84 modules with three separate voltages (V_{dda} , V_{dd} , and V_{dc}), and communication with the ATLAS Detector Control System is via a CAN bus interface. The station is approximately 10 meters from the detector, and each supply line is continuously sensed at the module to promptly adjust the output voltages, as necessary.

The core components of the Regulation Stations are printed circuit boards built on a highly dissipative substrate (approx. 10 W/board, see figure 2). Each board possesses 16 ST radiation-hard voltage regulators (LHC4913+) and provides roughly 1 A at 2 V, with 10 mV regulation steps, which is near the typical range of operation for the front end electronics (~ 2 V, ~ 1 A). All channels are floating up to ± 10 V. Programmable digital trimmers are addressed by control signals that are optocoupled to ensure isolation. Channels can be inhibited individually or per

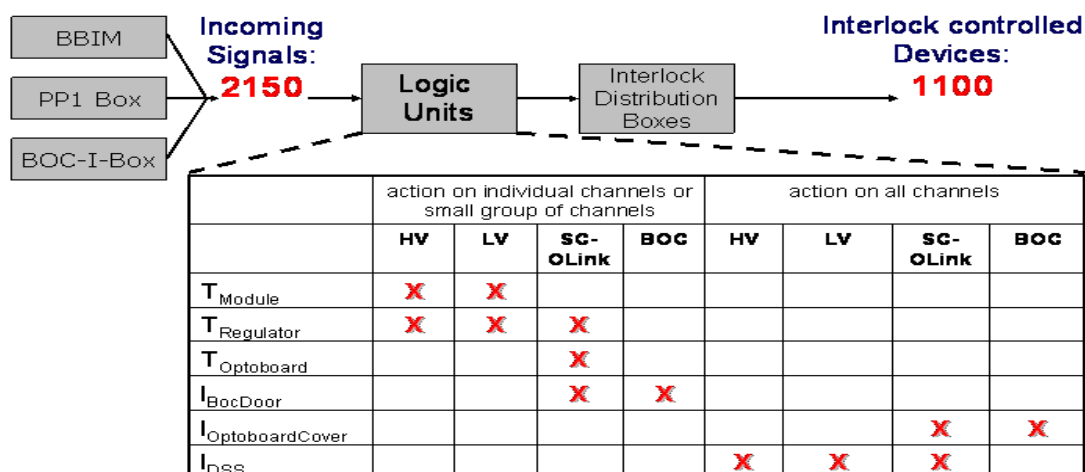


Figure 2. Schematic overview of the Interlock System and the action matrix.

board while kept floating. Further safety is provided by a current compensation on each channel, and protection of the output voltages against accidental disconnection of the sense lines.

All adjustment and monitoring functions in a Regulator Station are supervised by one controller board, which is based on an FPGA (APA075 from ACTEL, Mountain View CA, U.S.A.). The FPGA can be reprogrammed via CAN bus to facilitate operation during the ten year operation of ATLAS.

The need for programming the FPGA on demand derives from the fact that a degradation of the performances of the front end electronics is expected during the lifetime of the experiment. The full system has been irradiated and is rad-tolerant up to a NIEL $> 10^{12}$ 1 MeV_{neq}/cm².

5. Monitoring

5.1 Low voltage monitoring

A distribution of the low voltages is required as six or seven detector modules are supplied by one low voltage W.I.E.N.E.R power supply channel. This is performed by the patch panel 4, which are installed near to the low voltage crates. To have all information about the performance of each detector module, an additional current measurement per detector module is available. For debugging the system, especially to detect grounding problems, the current of the input and output lines can be measured.

The core components of the LV-PP4 are ELMBs. As with the SC-Olink, the use of optoisolators decouple the measuring circuits, which have a precision of between 2 to 10 mA over a range between 0 and 2 A.

Each LV-PP4 block can handle up to 28 supply lines and 56 measuring channels. The measuring channels are grouped in such a way that a second card with additional op-amps and optocouplers can be added should the measurement of the return current become necessary. In total, LV-PP4 will possess between 3500 to 7000 monitoring channels, the latter value corresponding to when all supply and return currents are measured.

5.2 High voltage monitoring

As the depletion voltage required by the pixel modules will increase during the detector lifetime, the modularity of the HV system will need to change. This not only affects the total

number of HV power supplies needed, but also the mapping of the power supply channels to the detector modules. This mapping is performed by the HV-PP4 crates.

The HV-PP4 provides a current measurement of the high voltage lines at the single module level (by the use of ELMBs), and also provides for the correct mapping of the *iseg* HV channels to the detector modules. 16 HV-PP4 crates will be required for the experiment, each with up to 117 monitoring channels. The large variation of the depletion current requires a substantial dynamic range of 0.4 mA to 4 μ A for these measuring circuits.

5.3 Building Block monitoring

About 2000 temperature sensors are required inside the pixel DCS. We have chosen 10 k Ω NTC (negative temperature coefficient) thermistors, as they combine radiation hardness (up to 10^{15} n/cm²), a large relative change of their resistance of 4%/K, and small SMD casings (0603). The humidity sensor Xeritron (from Hygrometrix, Alpine, CA, U.S.A.) has also been chosen because of its radiation hardness.

While the signals of the temperature sensors mounted on the detector modules, optoboards, and Regulator Stations are fed into the monitoring and Interlock System (see next section), all non-interlocked monitoring is handled by the BBM (Building Block Monitoring) crates [4]. This includes the humidity sensors and all temperature sensors which are installed inside the pixel volume in addition to those on the previously mentioned components.

The core of each BBM is again an ELMB which is used for the data readout, and with circuitry which has been specially adapted to supply NTC and Xeritron sensors and to handle their signals.

6. Interlock system

While the normal operation of the detector is steered by the DCS software, all situations in which safety is an issue are handled by the Interlock System. In order to prevent injury to people or damage to important parts of the detector, the hardware Interlock System is able to switch off all necessary power supplies and to operate completely independent from the rest of the control system.

Due to the dense circuitries of the front end chips, the power consumption inside the detector volume is very high. As higher temperatures for the detector modules lead to a faster ageing or, in extreme situations, can cause severe damage to the detector, their temperatures are monitored and, in parallel, the signals are fed into the Interlock System. As high temperatures are a risk to optoboards and Regulator Stations, as well, these units are also protected by the Interlock System.

One risk to people working in the counting rooms comes from the potential for injury of the eyes from the infra-red lasers employed by the optical links. Therefore, all lasers have to be switched off immediately in the event that one of the fibre connectors at either the detector or in the counting room side should be opened.

In the event of an interlock activation, the smallest necessary subset of power supplies is switched off in order to allow the rest of the detector to remain operational. In total the system handles 2150 incoming interlock signals and acts on 1100 interlock controlled devices. All circuits are built in negative logic; as soon as a cable is disconnected the related equipment is interlocked. An overview of the Interlock System is given in figure 2, while its components are described in more detail below [5].

6.1 Building Block Interlock and monitoring

The BBIM (Building Block Interlock Monitoring) crates receive the module, optoboard, and Regulator Station temperatures as analogue voltages. These are digitized by the BBIM's comparator circuits, called Interlock Boards, which have exchangeable threshold plug-ins, thereby providing the possibility to adapt to the needs of different equipment.

The digital information is then sent to the Logic Unit. In addition, the ELMBs which are housed in the BBIM monitor temperatures and deliver this information to the DCS software.

As the processing of the analogue signals should occur close to the detector, the BBIM crates are mounted in the environment of the ATLAS cavern, implying radiation exposure. Therefore, all components of the Interlock Board have undergone intensive radiation tests, and the required radiation tolerance criteria of 93 Gy and 5×10^{11} n/cm² (1 MeV) has been reached.

6.2 Logic Units

The Logic Units (LU) combine all of the 2150 incoming signals from the BBIM crates, the PP1 Boxes, the BOC-I-Box (BOC Interlock Box), and the DSS (Detector Safety System) into logical interlocks with a granularity of half staves and disk sectors. While the BBIM crates deliver the temperature alarms, the PP1 Box and the BOC-I-Box send signals when a part of the optical laser driven readout system is opened. In addition, DSS, an ATLAS wide system, provides an interlock signal in case of more general alarm conditions like smoke or a failure in the cooling system.

The core component of the LU is an FPGA (APA075) that determines the current situation from the input values and asserts the corresponding interlock alerts. The principle of its action matrix can be seen in figure 2.

Although the Interlock System is purely hardware based, it is required to communicate and explain the interlock actions to the rest of the DCS. This is realized by the use of ELMBs within the LU that read out the incoming signals and reports them to DCS. In addition, the digital outputs of the ELMB are used to provide test signals to the Interlock System.

6.3 Interlock Distribution Boxes

The IDB (Interlock Distribution Box) receives the logical interlock signals with a granularity of no more than seven modules, and distributes the interlock signals to the connected power supply channels in order to switch off the smallest possible subset of channels in the event of an interlock assertion. In total, 1100 devices are individually interlock controlled.

The IDB have the correct mapping of the power supplies, something which is complicated by the fact that the modularity of power supply channels connected to detector modules changes during the ten year lifetime of the detector. Further, the number of power supply channels per crate is different for low voltage, high voltage, and the SC-OLink, and cabling should be expected to change, as when single channels cease to function correctly. The flexibility needed to meet these requirements is achieved by the use of another FPGA (APA075).

An ELMB is used to monitor the interlock signals being forwarded to the power supplies. The combined information of the LU, IDB, PP1, and BOC-I-Box ELMBs ensures a consistent monitoring of all interlock activities.

7. Summary

The requirements of the pixel detector have made specific developments necessary for the hardware components of the power supply and detector control system.

Efficient operation requires the ability to make adjustments to each of the different control parameters. Further design constraints are the high power density in the detector volume, the floating grounding scheme requirement of the ATLAS detector, and the sensitivity of the readout chips developed in deep sub-micron technology. The power supply system in particular, consisting of nearly 5000 individually controllable supply lines, requires solutions which are adapted to the detector needs and which, in addition, are economically priced.

The remotely programmable Regulator Stations, which are installed as close as possible to the detector modules, provide individual floating power outputs with low ripple to the front end electronics. At the same time they protect the sensitive chips against transients. The internal control of the Regulator Station is handled by an FPGA from ACTEL, while the link into the control system is handled by an ELMB, which is the front end IO unit used throughout ATLAS.

The design of the supply system for the optical transceiver boards is based on components which can be directly controlled by the ELMB. In this manner a reasonably priced solution has been found which provides for the individual setting and adjustment of each of more than a thousand channels.

In those cases where common power supplies are used to provide voltages to several loads, additional monitoring units have been integrated which enable investigations of the behaviour of individual modules. The design constraints, precision requirements, and compatibility to the ATLAS grounding scheme are fulfilled by the low voltage monitoring system presented here. In the final system there will be more than 8000 monitoring channels in the low voltage and high voltage system.

As pixel detector module performance is very sensitive to temperature increases, especially after irradiation, a thermal Interlock System has been developed which acts directly on the related power supplies. In addition, other equipment can be damaged by extreme heat, and people must be protected from the risk of uncontrolled infrared lasers. Therefore, these devices are connected to the Interlock System as well. The interlock matrix presented here, with a design based on the use of FPGAs, provides dedicated control of small equipment groups and in this way keeps the number of channels out of service in the event of an interlock assertion as low as possible.

The hardware components discussed here have passed intensive electrical studies and investigation in our system tests and are currently under production.

A. Glossary

ATLAS	A toroidal LHC apparatus
BBIM	Building Block Interlock Monitoring
BBM	Building Block Monitoring
BOC	Back of crate card
CAN	Controller Area Network
DCS	Detector Control System
DSS	Detector Safety System
ELMB	Embedded Local Monitoring Board
FPGA	Field Programmable Gate Array
IDB	Interlock Distribution Box
LHC	Large Hadron Collider
LU	Logic Unit
MCC	Module Controller Chip

NIEL	Non Ionizing Energy Loss
NTC	Negative Temperature Coefficient
PP	Patch Panel
SC-OLink	Supply and Control for the Opto Link

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