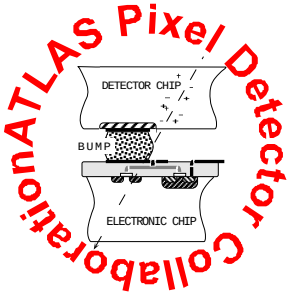
Pixel Detectors using MCM-D Technology



May 8th 1998

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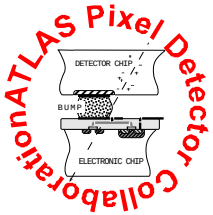
Workshop Pixel98

FNAL May 7-9th 1998

MCM-D, what‘s that ? (1)



- Thin film technology, integrating bus systems on a substrate
- Developement (a.o.) at
  - Interuniversity Microelectronics Center (**IMEC**, Leuven, Belgium)
  - Frauenhofer Institute for Reliability and Microintegration (**IZM**, Berlin, Germany)

MCM-D, what‘s that ? (2)

conductor layers

- Up to 5 copper layers:
  - magnetron sputtered
    up to 2 µm Ti/Cu/Ti
    ⇒ 10 mΩ/□
  - additive electroplating
    up to 5 µm Ti/Cu
- Minimal width and spacing
  15 and 20 µm
- Final metallisation:
  electroless
  5µm Ni:P/ 200nm Au

dielectric layers

- “Spin-on” polymer: BCB
  (Benzocyclobutene / DOW:CYCLOTENE™)
- Photosensitive
- Specific dielectric constant
  $\varepsilon_r = 2.7$
- Process temperatures :
  1h 220°C per layer
  last layer 1h 250 °C
- Thickness / layer 4 - 10 µm
- Via ∅ >20 µm, Pad 30µm

Structure of a Module **without** MCM-D

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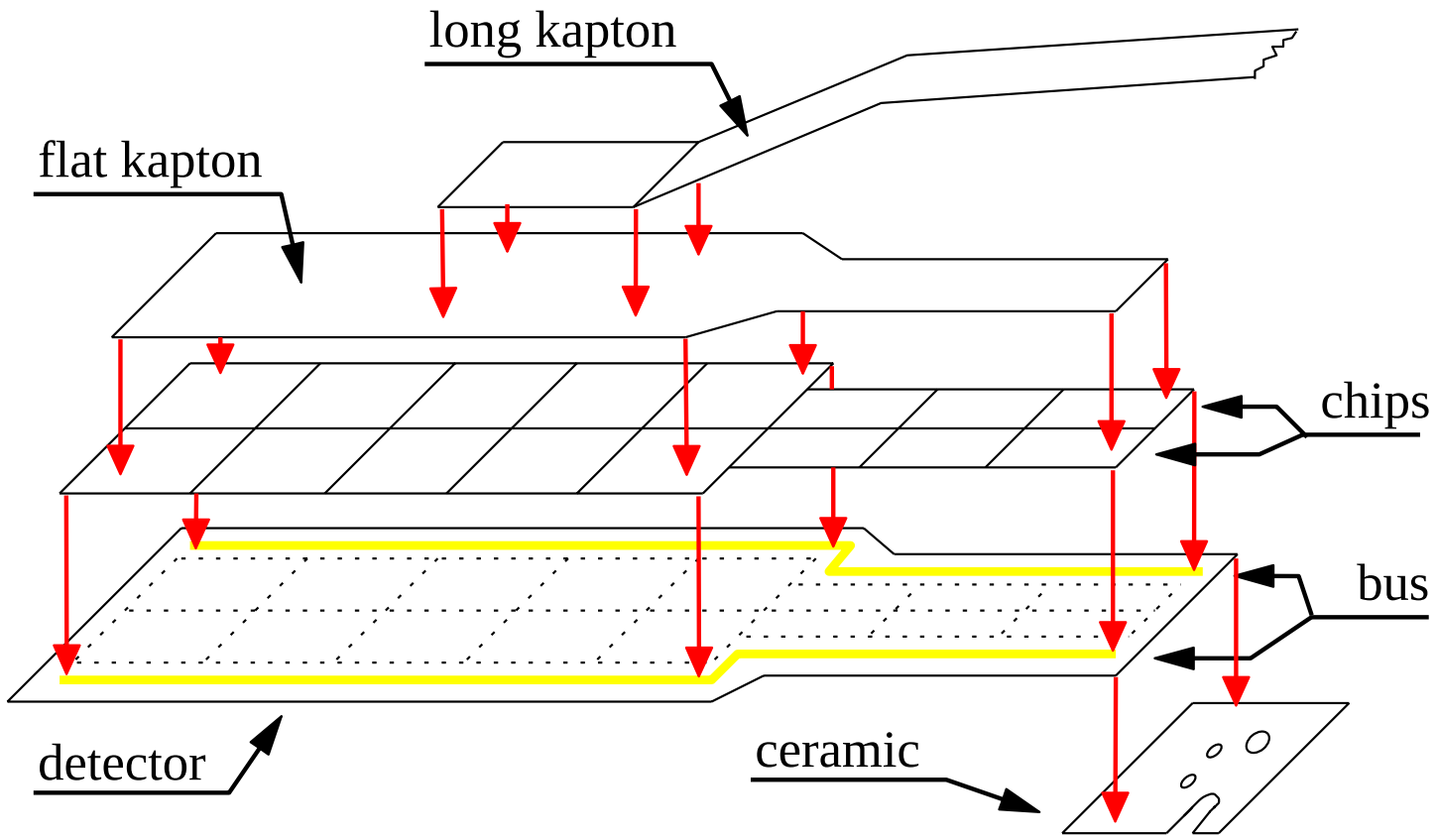
Example: DELPHI vertex detector pixel module (Raquette)



Structure of a Module **with** MCM-D

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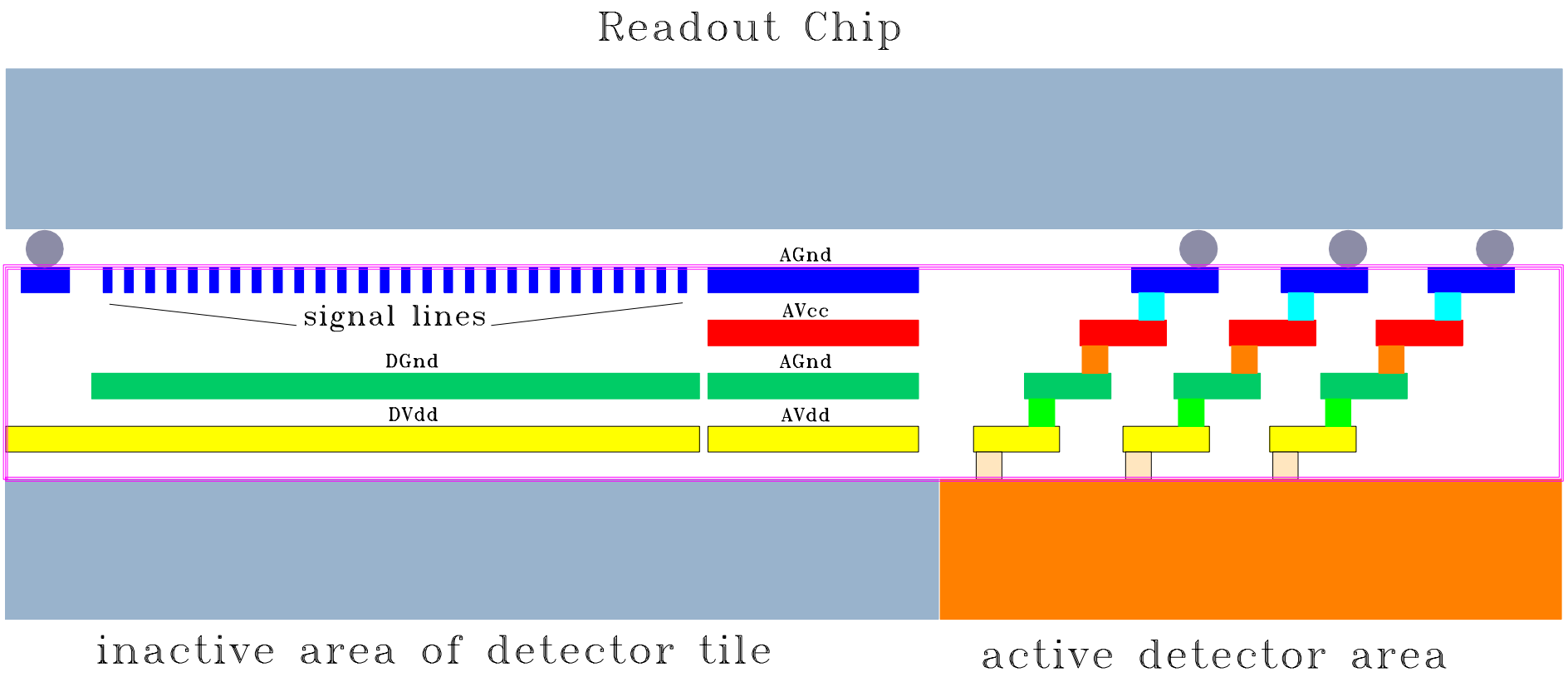
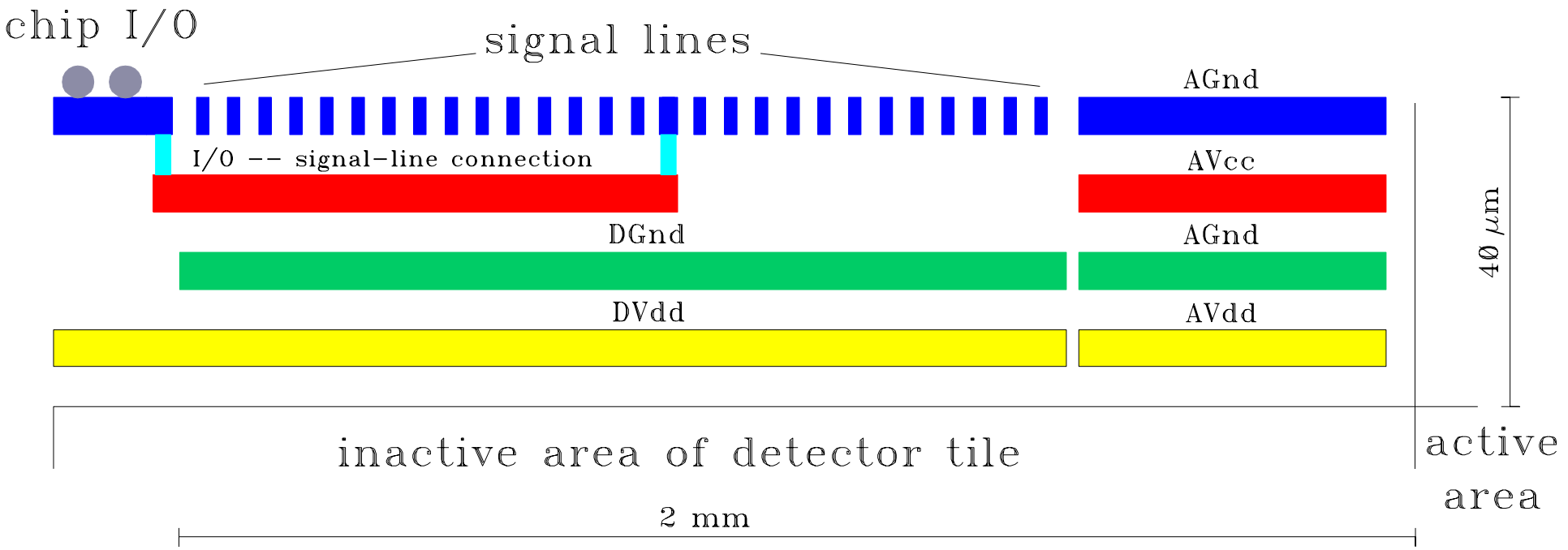


Cross-Section of a Bus System



Top View of a Bus System

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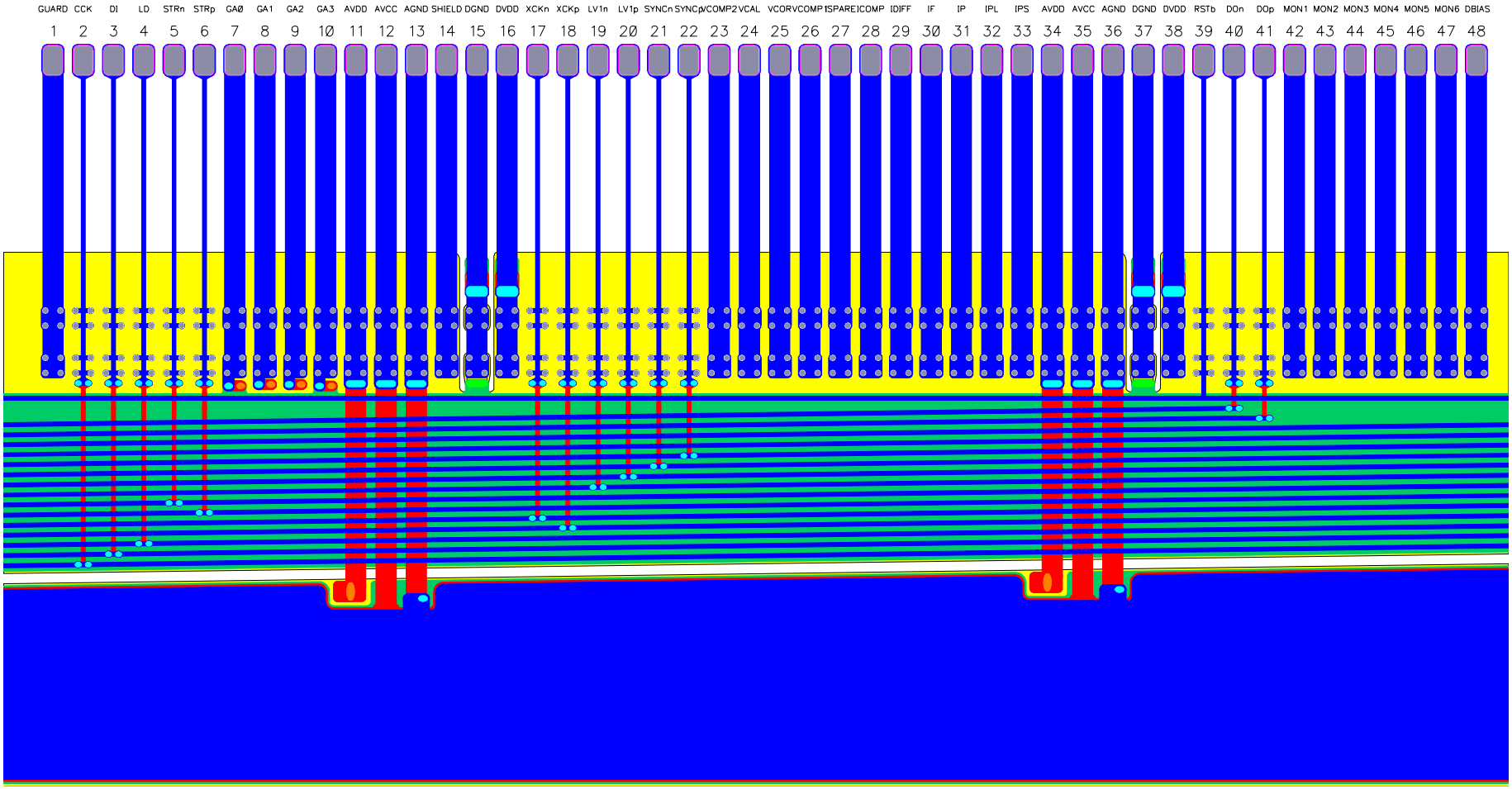


R&D Program

- ☑ Geometric requirements
- ☑ Radiation hardness
- ☑ Bump-bonding tests
- Test on active silicon
- Demonstrator module

Performance of the Bus System (1)

Bus system for 8 readout chips

Signal-Bus:

A 7cm long bus made of microstrip-lines 20 µm wide with 30 µm spacing shows

- Z_0= 68 Ω
- Crosstalk < 3%
- Signal-attenuation < 4 dB (<1GHz)

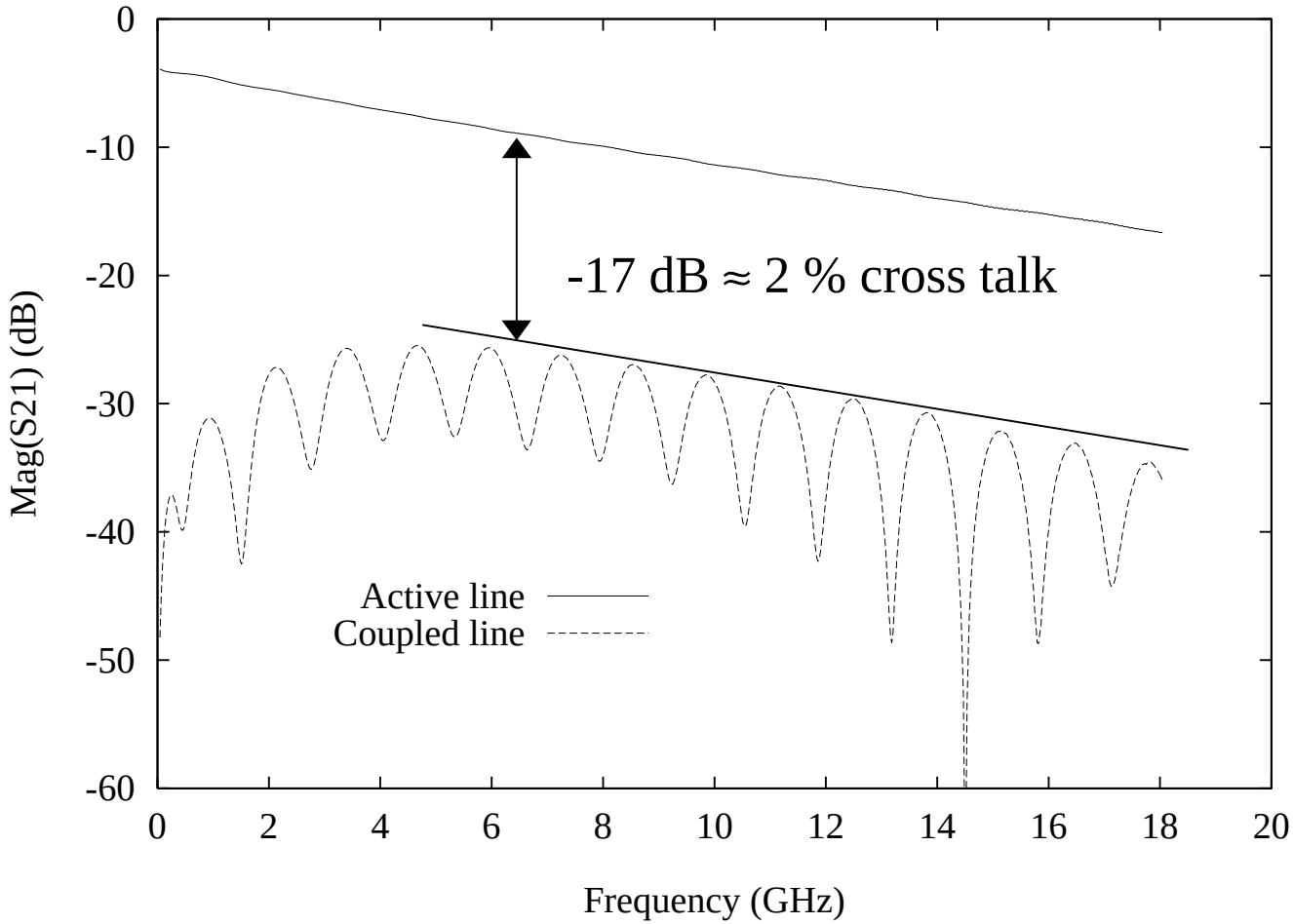
Power Supply Bus:

Calculations

⇒

- Power loss < 150 mW
- Max. difference of potentials 100 mV

Performance of the Bus System (2)



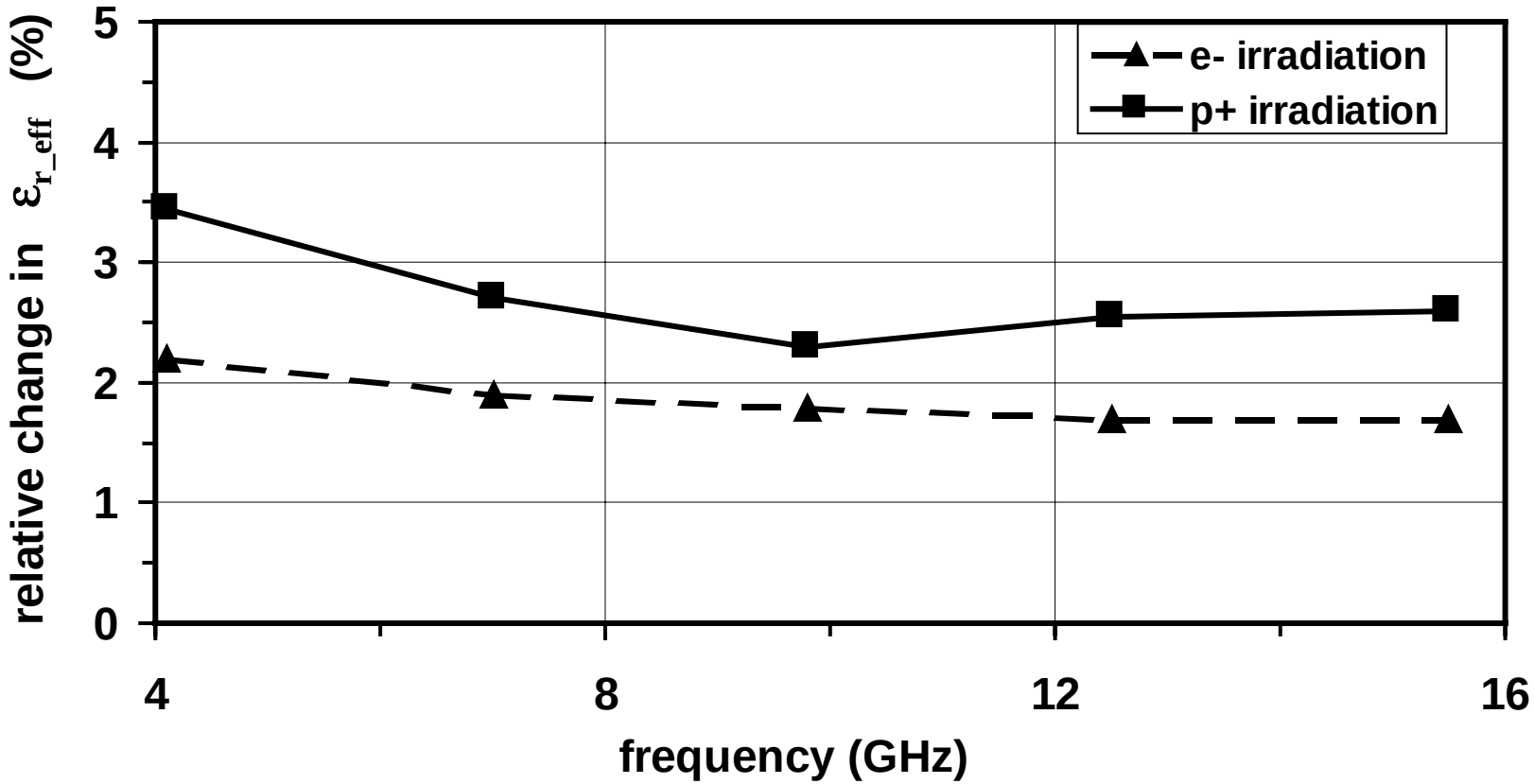
IMEC

Radiation Hardness (1)

- 10^{15} e^-/cm^2 at 40 keV cause a change in ε_{r_eff} of **2%.** **(Irradiation by C.Becker, Univ.Dortmund)**
- Irradiation of the same test-wafer with $5 \cdot 10^{14}$ p^+/cm^2 at 24 GeV protons causes a change in ε_{r_eff} in total of **3%.** **(Irradiation at CERN)**

⇨ *Due to absorption of moisture, a change in ε_{r_eff} of **1.4**% is expected.*

Radiation Hardness (2)



IMEC

Bump-Bonding Tests

- Two wafer layouts
  (detector and r/o-chips)
  with “daisy-chain” of bump connections
  (University of Bonn / IZM Berlin)
- $1.1 \cdot 10^6$ monitored vias with a diameter of 25µm indicating an error rate $< \mathbf{10^{-5}}$

Layout of a Feed-Through Structure

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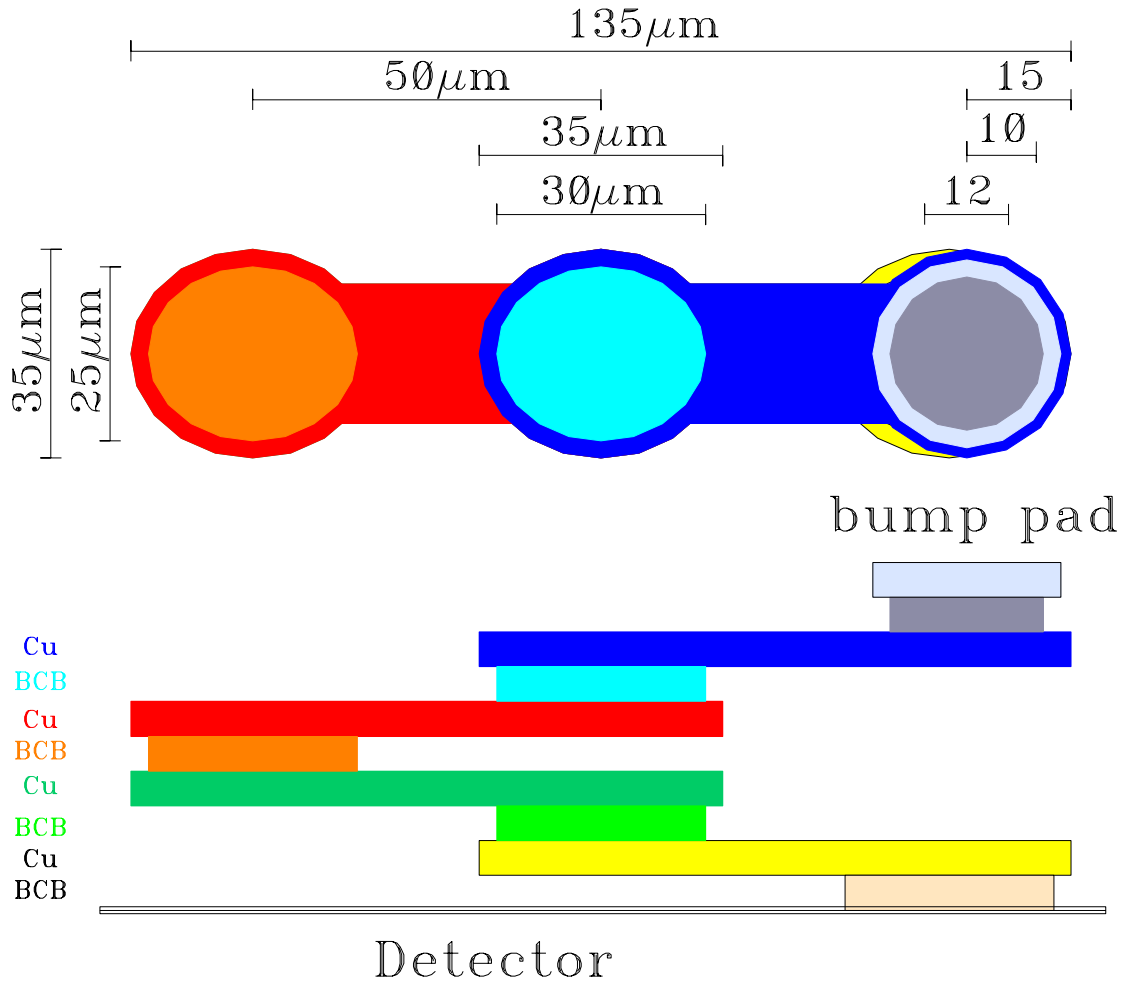
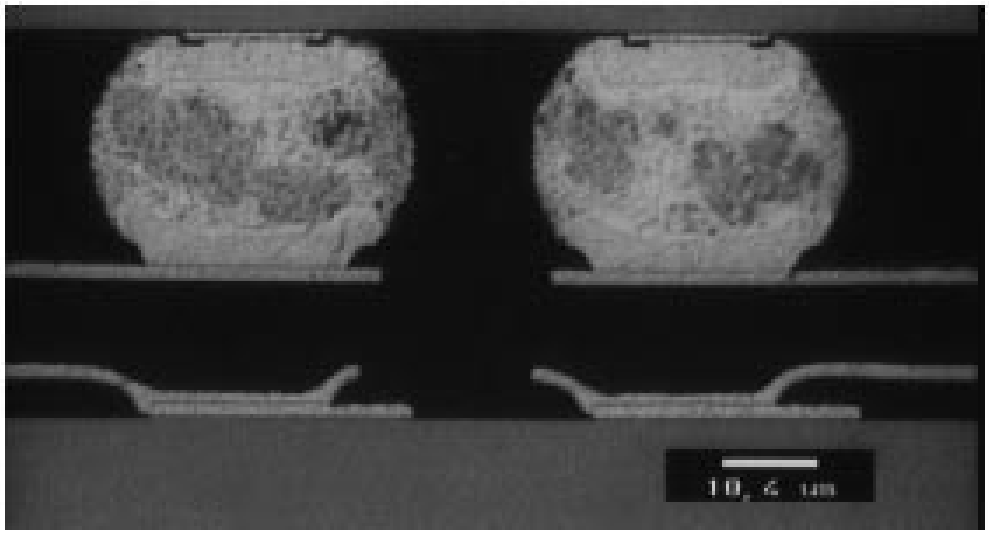
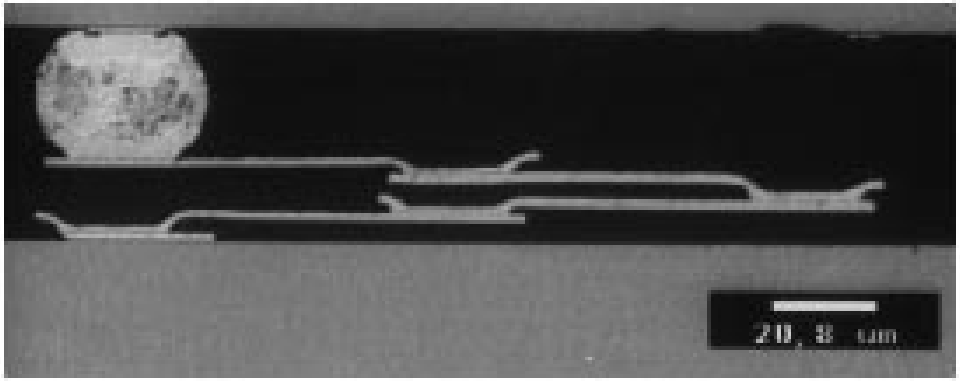


Cut through Bump Region

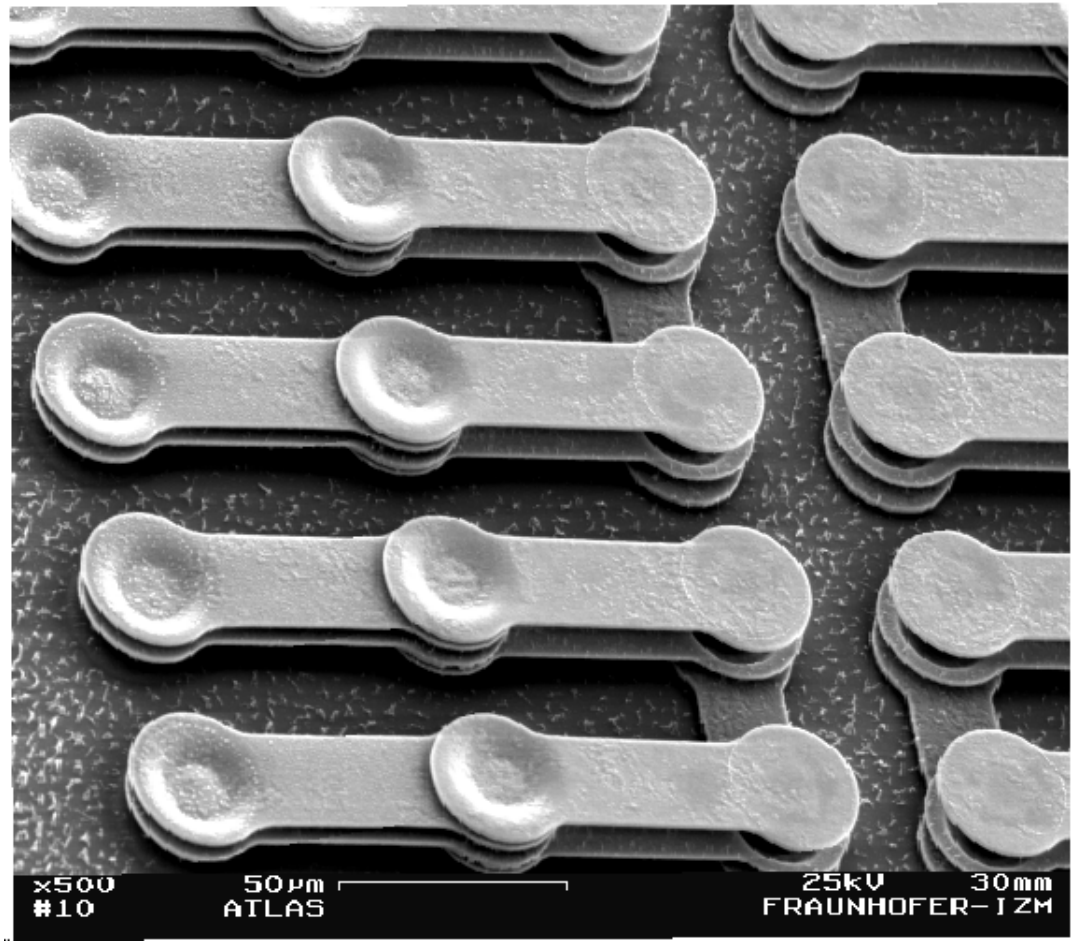


Photograph IZM



- Cross-section of flip chip bondet IC‘s on silicon substrate
- Bump pitch 50 µm
- 4 Cu layers and 5 Photo-BCB layers
  Photo-BCB: 5 µm thick, 25 µm vias

Feed-Through Structures



- Four copper layers
- BCB etched for better visualisation
- Measured defect rate

  $8.13 \cdot 10^{-6}$

  (9 defects in 1 105 920 vias)

Photograph IZM

Feed-Through Parasitics

- Resistance:
  - 2µm Cu-Layer ⇒ 10 mΩ / □
  - 5 mΩ per Via
  - ⇒ 60 - 160 mΩ per feed-through
- Coupling Capacitance:
  - 20 - 40 fF between 2 adjacent feed-throughs

Photograph of IZM MCM-D Prototype

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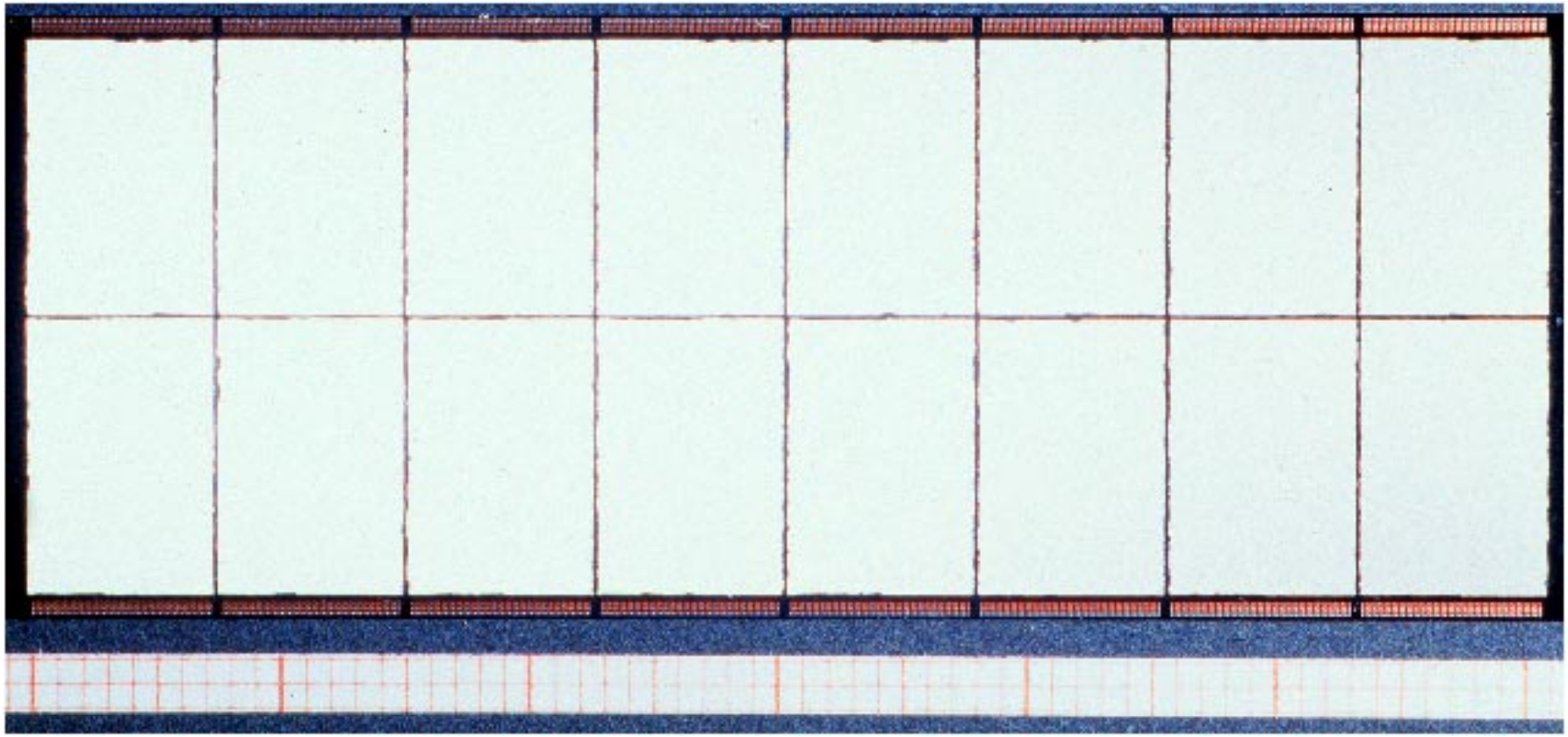

Multi Chip Module - Deposited Conclusions

radiation hard thin film technology

Up to **5 copper** layers

- Layer thickness up to **5 µm**
  (2µm Cu-Layer ⇒ 10 mΩ / □)
- Line width/pitch **20/50 µm**
- Impedance controlled

Benzocyclobutene (**BCB**)

- ε_r **= 2.7**
- Layer thickness **4 to 10 µm**
- Via down to ∅ **25 µm** (~1mil)
  failure rate **< 10^{-5}**

In progess:

- Test on active silicon
- Demonstrator module