

First MCM-D Modules for the B-Physics Layer of the ATLAS Pixel Detector

O. Bäskén¹, K.-H. Becks¹, O. Ehrmann², P. Gerlach¹, Ch. Grah¹, I.M. Gregor¹,
Ch. Linder¹, S. Meuser³, J. Richardson⁴, M. Töpfer², and J. Wolf²

for the ATLAS Pixel Collaboration

¹Physics Department, University of Wuppertal, Germany

²Fraunhofer Institute - IZM, Berlin, Germany

³Physics Department, University of Bonn, Germany

⁴Lawrence Berkeley National Laboratory, Berkeley, USA

Abstract

The innermost layer (b-physics layer) of the ATLAS Pixel Detector will consist of modules based on MCM-D technology. Such a module consists of a sensor tile with an active area of 16.4 mm x 60.4 mm, 16 read out ICs, each serving 24 x 160 pixel unit cells, a module controller chip (MCC), an optical transceiver and the local signal interconnection and power distribution busses. Figure 1 shows a prototype of such a module with additional test pads on both sides. The outer dimensions of the final module will be 21.4 mm x 67.8 mm. The extremely high wiring density, which is necessary to interconnect the read-out chips, was achieved using a thin film Copper/Photo-BCB process on the pixel array. The bumping of the read out chips was done using electroplating PbSn. All dice are then attached by flip-chip assembly to the sensor diodes and the local busses. This thin film technology has been described in [1] and is under further development at Fraunhofer-IZM in Berlin. Focus of this paper is the description of the first results of such MCM-D-type modules.

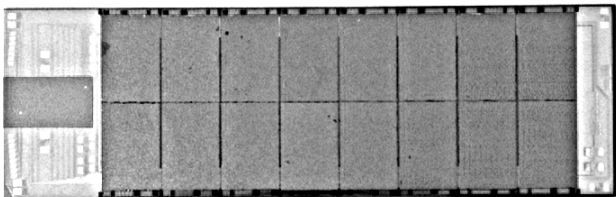


Figure 1: Photograph of a prototype MCM-D Pixel Module

I. THE MCM-D TECHNOLOGY

All electronic chips are located in the same plane. The data lines, control lines and power distributions are routed to the periphery of the module, to a module controller chip and a power distribution cable and optical fibres for data transmission.

All interconnections are made using Multi Chip Module Deposited technology (MCM-D), solder bump connections and flip-chip assembly. The interconnection lines are formed by depositing dielectric materials and conductors onto a base substrate, in our case the high resistivity silicon sensor. A four-layer thin film metallisation is necessary to route the power, ground and signal layers. The signal lines were designed in microstrip line configuration. All sensor elements have to be connected to their corresponding read-out cells by small pitch via connections through the four layers. This was only achievable by the depicted multilayer metallisation scheme. A mini-

imum of 25 μm for the diameter of these so-called vias was allowed by the design rules. On the other side a minimum of 3 μm thick isolation between the metal layers was demanded. Three μm copper was electroplated for the metallisations [2]. Figure 2 shows a schematic cross section of this layout.

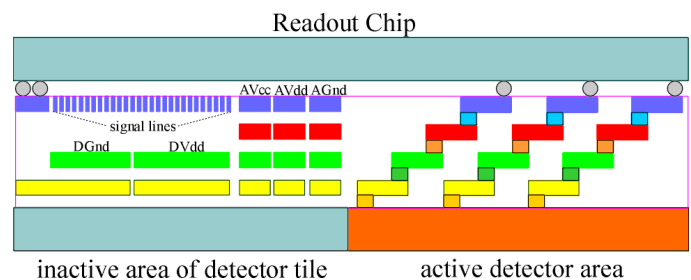


Figure 2: Schematic cross section of the four-layer bus and signal system. On the right-hand side the feed through connections from the detector to the readout chip are illustrated.

This four Cu layer bus system for an ATLAS module is situated below the end-of-column logic of the front-end chips. This in turn is situated within the outermost 2 mm on both long sides of the inactive area of the sensor.

II. FEASIBILITY STUDIES

High frequency tests, cross talk measurements and irradiation tests have shown the feasibility and good performance of this kind of signal and bus system [3]. In order to check if the sensor tile is affected by the processing procedure, the sensor

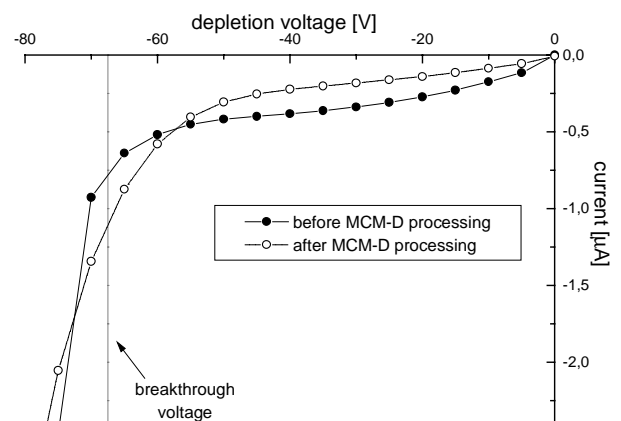


Figure 3: IV characteristics of the sensor tile before and after processing.

leakage current was measured before and after the processing steps. Figure 3 depicts the measurements exemplary for one sensor tile. Within the measuring tolerances both curves agree. For both measurements the breakthrough voltage is about -70V. In conclusion, the sensor properties are not affected by the MCM-D processing.

III. SINGLE CHIP MODULE (SCM-D)

A single chip module consisting of a sensor cell array and a so-called front-end chip (FeB [4] or FeC [5]) with MCM-D interconnections has been set up to measure the electrical properties of this technology.

The front-end chips provide an amplifier, a discriminator and a digital readout logic for each sensor cell. Therefore a binary readout is used. This is achieved by comparing the amount of charge collected by a sensor cell with a threshold value set in the discriminator of the front-end chip. Only a charge above this threshold is declared to be a hit and its coordinates are collected in a memory buffer together with a time information. If a corresponding trigger signal is received, the coordinates are transferred to the module controller chip (MCC), sorted and uploaded to a read out driver [6]. The behaviour of the analog parts of the front-end chips is controlled by several digital to analog converters on the chips themselves. The threshold of the discriminator is tuneable for each pixel individually.

A. Threshold and Noise Measurements

Special circuitry in each pixel enables the injection of charge into selected pixels. This gives the possibility to measure the threshold of the discriminator and the noise of the system.

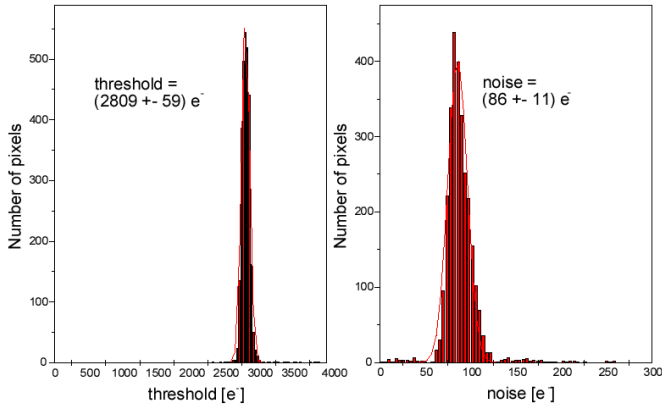


Figure 4: Threshold and noise distribution of a single chip (here FeC).

The threshold distribution of the front-end chip (FeC) is shown in figure 4. The mean values of around 2800 electrons with a spread of ± 60 electrons are very consistent with the typical threshold of <3000 electrons and a spread of less than 200 electrons of non-MCM-D single chip modules.

The MCM-D structures connecting sensor and readout cells introduce additional coupling capacitances between the sensor elements. The results indicate that this effect causes nearly no changes in the overall system performance.

B. Routed Pixel and Crosstalk Measurements

In the “classical” approach for a hybrid pixel detector the geometry of the sensor cells and the electronic cells have to be congruent. Due to the additional freedom in the routing of the interconnections when using MCM-D technology, it is possible to optimise the geometry. Bricked and equal sized pixel become possible.

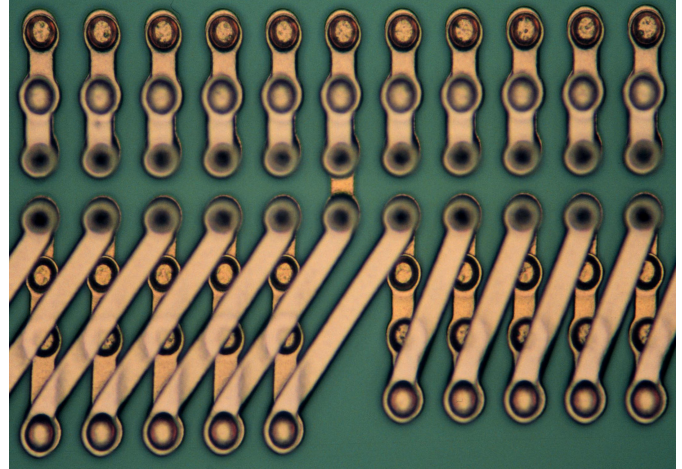


Figure 5: Upper Row: Unrouted pixel class “U”. Lower right: class “R1”. Lower Left: class “R2”.

Three different types of routed pixel were designed to test the routing capabilities and their influence on the performance of the system. For the “R1” type of routed pixel the routing connects the sensor cell with the neighbouring electronics cell (figure 5). If one cell is skipped and the sensor cell is routed to the second neighbour, the type is called “R2”. In the “R3” class the sensor cell is routed to the third neighbour.

The crosstalk between pixel cells is defined as the fraction of charge that couples into the neighbouring pixel through the interpixel capacitance. This can be measured by injecting a large charge Q into a pixel N , which is masked to read out. The charge Q_c at which the neighbouring pixel $N+1$ reports hits is compared to the fixed threshold value T of its discriminator. The crosstalk is defined as T/Q_c . Due to additional capacitances through the crossing lines more pickup and crosstalk is possible. Table 1 shows the results of the three types of routed pixels for sensors with FeB and FeC chips. All measurements were done with a so-called ST1 sensor [7], a special prototype sensor for the Pixel Detector. For unrouted pixels (class U) the crosstalk in the adjacent pixel is about 2,5% (FeB) respectively

Table 1
Crosstalk for the three types of routed pixel

neighbouring pixel	Class U	Class R1	Class R2	Class R3
nearest FeB	2,5%	3,0%	3,4%	3,4%
FeC	7%	8,2%	8,9%	8,5%
2 nd FeB	1%	1,0%	1,4%	1,8%
FeC	2%	2,8%	4,3%	5,6%
3 rd FeB	<1%	<1%	<1%	1,1%
FeC	<2%	<2%	<2%	2,9%

7% (FeC). The front-end chip C is more sensitive to crosstalk.

The results show that the routing of the interconnections does not significantly influence the performance of the electronics. Without routing (class U) the crosstalk corresponds to values measured with non-MCMD hybrid.

C. Test Beam Measurements

For the test beam measurements the detector system is placed into a reference system (*beam* telescope) and used to detect high energy particles produced by an accelerator. A single chip in MCM-D technology has shown good results in a test beam at CERN.

As an example, results for a MCM-D single chip module with FeB in the so-called "small gap design" are presented [9]. Figure 6 shows the resolution in the short pixel direction for single hits. The plot illustrates the difference between the expected and the measured positions.

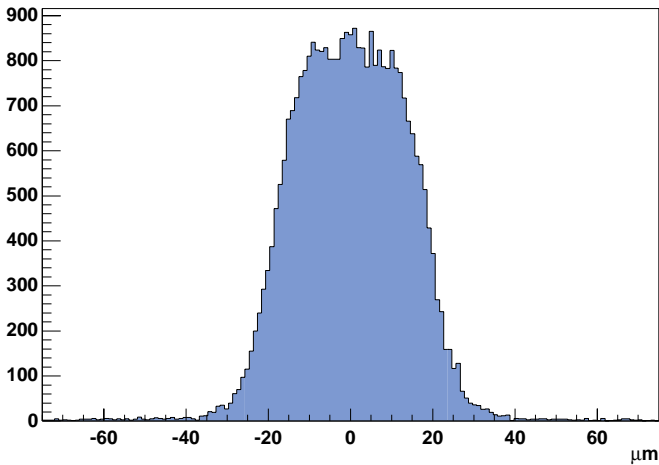


Figure 6: Residuals expected – measured position for single hits

For single pixel hits the assumed position is the centre of the hit pixel. The abscissa of the histogram corresponds to the width of three pixels, each 50 μm wide. As expected, one observes a flat plateau of about 30 μm, which is related to hits around the centre of the pixel. The edges correspond to hits

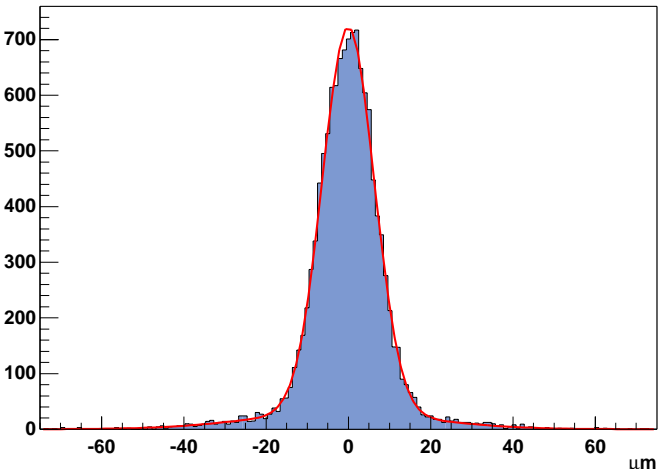


Figure 7: Binary double hit resolution. With this method one achieves a resolution of $\sigma = 6.3 \mu\text{m}$.

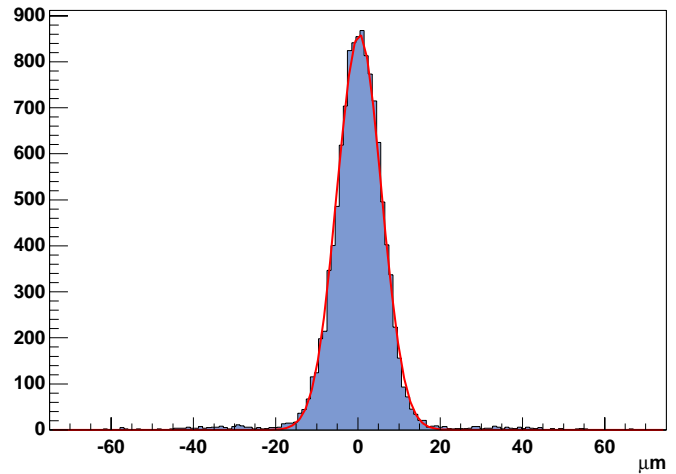


Figure 8: Analog double hit resolution. With this method one achieves a resolution of $\sigma = 5.4 \mu\text{m}$.

near the borders of the pixel, where the probability for double hits increases. Compared to non MCM-D structures the width of the plateau is narrower. This is due to higher crosstalk between neighbouring pixels, increasing slightly the number of double hits.

Figures 7 and 8 show the resolutions for double hits, where the charge created by a crossing particle is distributed on two pixels. The first histogram (figure 7) includes the so-called "binary" information, i. e. only the centre coordinates of the hit pixels are taken into account to calculate the position of the track interception. One observes broad tails, which are due to the crosstalk. For the comparison with non MCM-D structures, two Gaussians are fitted, one for crosstalk effects and one for the resolution. One achieves a resolution of 6.3 μm, which is the same as for non MCM-D structures [10,11]. In the second histogram (figure 8) we use the TOT (time over threshold) information to correct the position of the particle interception. The TOT is the time the output signal of the preamplifier is above a given threshold. It is proportional to the charge collected in the sensor cell. Using the TOT-weighted positions, the resolution decreases to 5.4 μm. Furthermore the tails due to the crosstalk are suppressed. Hits generated due to crosstalk have small signals above the threshold and therefore only small contributions to the weighting algorithm. In conclusion, the test beam measurements with MCM-D single chips compared to non MCM-D chips show the same results for the resolution. Further studies concerning the crosstalk and charge collection efficiency are under investigation.

IV. FULL SCALE MODULE (MCM-D)

In co-operation with IZM first full scale MCM-D prototype modules have been built. Each of these modules includes a four-layer system for all power and digital (inter-)connections for the 16 front-end chips (in this case FeB) and the module controller chip. All dice are completely connected through solder bumps. Overall, this prototype module provides 46.080 pixel cells, more than 48.000 bump bonds and more than 185.000 vias (connections between two copper layers through one BCB layer).

Two different kinds of measurements are shown here to describe the performance of this system.

A. Threshold and Noise Measurements

In figure 9 the threshold and noise distributions of all 16 chips are shown.

The measurements were done with the default settings of the DACs in the front-end chips and pixels. The threshold and noise distributions indicate that the overall performance of a module is not reduced by the MCM-D technology. A further adjustment of the electronic parameters will result in more uniform and lower thresholds. The measurements are not completed yet.

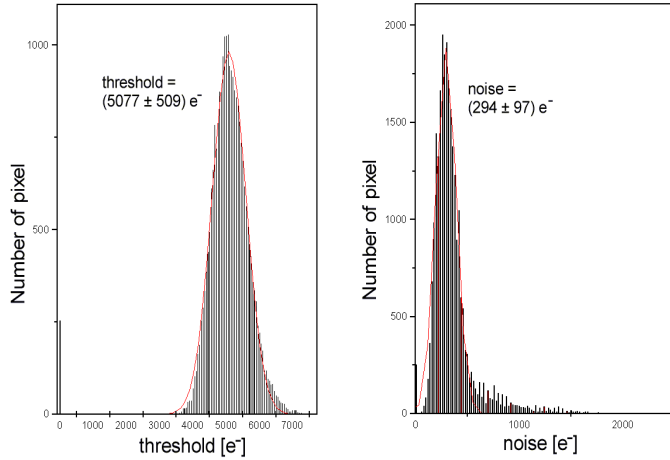


Figure 9: Threshold and noise distribution of a full scale MCM-D module.

B. Source Measurements

In the laboratory, tests with radioactive sources have been performed to get information about short circuits, dead pixel or failed solder bump connections. The source has been placed above the module and the response of the pixel was taken. The hitmap of a ^{241}Am measurement in figure 10 shows the response of chip #7 of a full-scale module. The black pixels on the top are intentionally left dead. This is due to the routing described in III.A

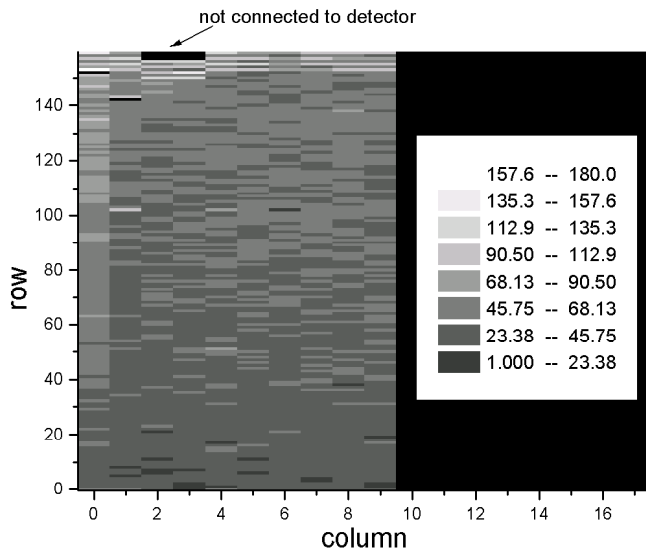


Figure 10: Hitmap of a source measurement with ^{241}Am .

V. CONCLUSIONS

This Paper discusses the performance of the first ATLAS pixel detector Multi Chip Modules built using metal and insulator depositing techniques (MCM-D).

From the presented results it can be concluded that the depositing technique is able to implement pixel detector modules as needed for high-energy collider experiments. It could be shown that the high resistive sensor material, which is used in this approach as the thin film layers substrate is not damaged by the depositing process. First prototypes of a geometry based on ATLAS prototype sensors and readout chips have been successfully built. Laboratory and test-beam measurements on Single Chip Modules show only a negligible influence of the needed metal structures on threshold and noise performances. The measured crosstalk is only marginally increased and has no impact, as can be seen in the resolution measurements.

The usage of the MCM-D technology gives the freedom to optimise the segmentation of the sensor regardless of the pitch given by the readout electronics. This option, which allows equal sized or "bricked" pixel cells, is being investigated with special structures on the existing devices. The laboratory tests on these structures were shown and give very encouraging results. Full-scale modules have been built as well, including 16 readout chips and a module controller chip. It could be demonstrated that the proposed signal and power distribution systems worked as foreseen. This shows the feasibility to implement such devices in MCM-D technology.

In the near future, the full scale modules will be adapted to the next generation of electronic chips and sensor prototypes and the module connections to the outer world will be implemented in a more realistic way including an optical-link. With these devices, the problems of a higher volume production will be studied.

VI. ACKNOWLEDGEMENTS

The content of this paper documents only a small part of the results achieved by the ATLAS Pixel Collaboration (CERN). Many more people than listed above contributed with their help, knowledge and time. The authors would like to thank C.Göbbling, F.Hüging, J.Wüstenfeld and R.Wunstorf (University of Dortmund, Germany) for their help with all sensor concerned measurements and questions. Many thanks also apply to M.Keil and N.Wermes (University of Bonn, Germany) for their support in the measurements of the FeC-chips and the first fully equipped module, and K.Einsweiler (LBL, USA) for his help concerning all FeB-chip questions and their results with FeB-SCMD's.

A real great effort and success has been achieved by the whole crew of the testbeam consisting of a huge part of the collaboration, especially P.Delpierre and J.-C.Clemens (both CPP Marseille, France).

VII REFERENCES

- [1] K.-H. Becks et al., "A Multi-Chip Module, the Basic Building Block for Large Area Pixel Detectors", Proc. of IEEE Multi-Chip Module Conference (1996) 16.
- [2] M. Töpper et. al., "Fabrication of a High-Density MCM-D for a Pixel Detector System using a BCB/Cu Technology", Proc. of the International Conference on High Density Packaging and MCMs, Denver, Colorado (April 1999)
- [3] K.-H. Becks et al., "A MCM-D type module for the ATLAS Pixel Detector", Proc. of IEEE Nuclear Science Symposium, Toronto, Canada (1998).
- [4] K. Einsweiler et al. "On the Performance and Limitations of a Dual Threshold Discriminator Pixel Readout Circuit for LHC", Proc. of IEEE Nuclear Science Symposium, Toronto, Canada (1998).
- [5] S. I. Meuser , "Pixel Readout Chip for the ATLAS Experiment", Proc. of IEEE Nuclear Science Symposium, Toronto, Canada (1998).
- [6] R. Beccherle, "The Module Controller Chip (MCC) of the ATLAS Pixel Detector", Proc. of IEEE Nuclear Science Symposium, Toronto, Canada (1998).
- [7] M.S. Alam et al. "The ATLAS Silicon Sensors", ATL-INDET-99-012, (9/1999) Submitted to Nucl. Instr. and Meth. A.
- [8] ATLAS Inner Detector, Technical Design Report, Vol. II, CERN/LHCC/97-17 (1997).
- [9] ATLAS Pixel detector, Technical Design Report, CERN/LHCC/98-13, (5/1998).
- [10] F. Ragusa, "Recent Developments in the ATLAS Pixel Detector", talk given at the 8th International Workshop on Vertex Detectors, VERTEX 99, 20-25 June 1999, Texel, Netherlands, to be published on Nucl. Instr. and Meth. A.
- [11] C. Troncon, "Detailed Studies of the ATLAS Pixel Detector", sub. to the IEEE Nuclear Science Symposium Proc., October 99 Seattle, Washington.