

CPLD Testpoints	RX0				RX3				RX4				RX7			
	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D
Testmode																
0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
1	-	Dout0_1	Dout0_0	Din0	-	-	-	-	-	-	-	-	DX1out0_0	-	DXout2_0	Din0
2	Dout0_3	Dout0_2	0	Din1	-	-	-	-	-	-	-	-	DX1out0_1	-	DXout2_1	Din1
3	Dxout1_0	Dout1_1	Dout1_0	Din2	-	-	-	-	-	-	-	-	Dxout2_2	-	DXout2_2	Din2
4	Dxout1_3	Dout1_3	Dout1_2	Din3	-	-	-	-	-	-	-	-	Dxout2_3	-	DXout2_3	Din3
5	Dxout1_0	-	DXout1_0	Din4	-	Dout2_9	Dout2_8	Dxin0_0	DX1in0_1	Dout4_1	Dout4_0	Dxin3_0	Dxout2_0	Dout6_9	Dout6_8	Din4
6	Dxout1_1	-	DXout1_1	Din5	DX1in3_0	Dout2_B	Dout2_A	Dxin0_1	Dxin3_0	Dout4_3	Dout4_2	Dxin3_1	Dxout2_1	Dout6_B	Dout6_A	Din5
7	DX1out3_0	-	DXout1_2	Din6	Dxin0_1	Dout3_1	Dout3_0	Dxin0_2	DX1in0_0	Dout5_1	Dout5_0	Dxin3_2	-	Dout7_1	Dout7_0	Din6
8	DX1out3_1	-	DXout1_3	Din7	DX1in3_1	Dout3_3	Dout3_2	Dxin0_3	Dxin3_1	Dout5_3	Dout5_2	Dxin3_3	-	Dout7_3	Dout7_2	Din7
9	Dout0_3	Dout0_2	Dout0_1	Dout0_0	Dout2_B	Dout2_A	Dout2_9	Dout2_8	Dout4_3	Dout4_2	Dout4_1	Dout4_0	Dout6_B	Dout6_A	Dout6_9	Dout6_8
10	Dout1_3	Dout1_2	Dout1_1	Dout1_0	Dout3_3	Dout3_2	Dout3_1	Dout3_0	Dout5_3	Dout5_2	Dout5_1	Dout5_0	Dout7_3	Dout7_2	Dout7_1	Dout7_0
11	Dout0_1	Dout0_0	Din1	Din0	Dout2_9	Dout2_8	Din1	Din0	Dout4_1	Dout4_0	Din1	Din0	Dout6_9	Dout6_8	Din1	Din0
12	Dout0_3	Dout0_2	Din3	Din2	Dout2_B	Dout2_A	Din3	Din2	Dout4_2	Dout4_3	Din3	Din2	Dout6_B	Dout6_A	Din3	Din2
13	Dout1_1	Dout1_0	Din5	Din4	Dout3_1	Dout3_0	Din5	Din4	Dout5_1	Dout5_0	Din5	Din4	Dout7_1	Dout7_0	Din5	Din4
14	Dout1_3	Dout1_2	Din7	Din6	Dout3_3	Dout3_2	Din7	Din6	Dout5_3	Dout5_2	Din7	Din6	Dout7_3	Dout7_2	Din7	Din6
15	-	Dout1_1	Dout1_0	Din1	-	Dout3_1	Dout3_0	Dxin0_1	-	-	-	-	-	-	-	-

Important Note: the yellow rotari switch is behaving inverted to the red one (Yellow 0xF is Red 0x0 and so on). The table is given for the red one.
 red rotari switches on BOC 0x0 – 0x5, red rotari switches on all the other BOCs

Nomenclature: Din<n> 8 inputlinks of the RX-plugin (0..7)

Dout<Formatter[0..7]><Channel[0..B]>

Piggyback V2 Dxout<Destination CPLD><stream> cross connections between the CPLDs
 Dxin<Sender CPLD><stream>

Piggyback V1 DX1out<Destination CPLD><stream> cross connections between the CPLDs
 DX1in<Sender CPLD><stream>

All the Dx's are just for check of the BOC internal routing,
 for output to ROD look at Dout's
 for input to BOC look at Din's