BOC Parameter Description

There are several parameters on the Back of Crate card: clock-controls, clock-delays, data-delays, plugin parameters, mode parameters. A short description of the different parameters will be given here.

Clocks:

5 different clocks are on the BOC: ROD-clock, A-clock, BPM-clock, B-clock, V-clock. While the ROD clock is a direct copy of the system clock given to the ROD and the A-clock is the clock to make the on BOC chips working, the three other clocks may be controlled for the module and data operation with several parameters:

Clock-control-register [4..0]:

bit	**description**
0	V-clock invert
1	half V-clock
2	Vernier Step bypass
3	BPM-delay bypass
4	Phos4 clock / 4 (for Reset of Phos4 chips)

BPM-Clock-delay [0x0..0x18]:
gives the delay from 0..24ns for the BPM-clock in 1ns steps

B-Clock-delay [0x0..0x18]:
gives the delay from 0..24ns for the B-clock in 1ns steps

V0-Clock-delay [0x0..0x18]:
gives a delay from 0..24ns for the V-clock in 1ns steps

V1-Clock-delay [0x0..0x18]:
gives a delay from 0..24ns for the V-clock in 1ns steps
one may add V0 and V1 to get a delay of 48ns.

V-Clock-finedelay [0x0..0xFF]:
gives the delay from 0..10.2ns for the V-clock in 40ps steps. (in principle not used for pixels)

RX-plugin parameters:

There are two parameters per RX-channel, the RX-Threshold and the RX-Delay. The threshold is action directly on the plugin via the MDACs while the delay is done in the data path between the plugin and the CPLDs by Phos4 chips.

RX-data-delay [0x0..0x18]:
gives the delay from 0..24ns for the data in 1ns steps. Can be done channelwise.

RX-threshold [0x0..0xFF]:
controls the discriminator threshold of the DRX-chip on the RX-plugin. The higher the values the higher the threshold. (Channelwise)

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The parameters on the TX-plugin are on the one hand the laser currents for the VCSEL channels and on the other hand the BPM parameters, like coarse and fine delay and inhibit and mark space ratio.

BPM-coarse-delay [0x0..0x1F]:
is delaying the signal going to the module between 0..775ns in 25ns steps (channelwise).

BPM-fine-delay [0x0..0x7F]:
can delay the signal going to the module between 0..63.5ns in 0.5ns steps (channelwise).

BPM-inhibit [0x0..0x1]:
Normal data mode is 0x0. Setting the inhibit (0x1) is preventing the BPM to decode the data into the stream. Only the clock is decoded. This results in a 20MHz clock like BPM-signal. This is useful for resetting the Optoboard which needs a „only clock“ BPM-signal while resetting.

BPM-mark-space-ratio [0x0..0x18]:
The mark-space ratio is giving the balance of the high/low signal length. It should be set like that the signal is balanced 50:50. The laser current and the BPM-fine-delay have influence on this ratio as well.

Laser current [0x0..0xFF]:
the amount of current going to the VCSEL channel. Its 0mA up to 150 and then linear to around 18mA at 255.

BOC modes:

The BOC is able to work in different modes adopted to the functionality is may serve. There is the RX-mode register to write in and set the different modes.

RX-mode register [0x0..0x7]:

Mode	Description
0	Pixel Layer 2 (40Mb/s) remapped
1	Pixel B-Layer Mode (2*80Mb/s, Disk/L1 Optoboard, piggyback V1)
2	Pixel Disk & B-Layer Mode (2*80Mb/s, B-Layer Optoboard, piggyback V2)
3	Same as Mode 2, but EVEN/ODD BIT (or output streams) SWAPPED
4	Phos4 clock test route 0
5	Phos4 clock test route 1
6	CLOCK as DATA
7	TRANSPARENT MODE (no CPLD sampling of the data)