BoC card installation and control description

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Nov 2004

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Abstract

This article should give a short overview how to install and handle a Back of Crate card in the read out chain for the ATLAS pixel detector. Some information about the optoboards are included, too.

Chapter 1

The Back of Crate card installation and handling

1.1 Installing the Hardware

The Back of Crate card will be installed on the back side of the crate. If there is no special backplane installed a back to back connector should fit in vme plug 3. To this connector (pin A21 and D11) the laser interlock will be connected.

The TX- and RX-boards are installed onto the BOC. Be aware in case of B-Layer modules running at 160 MHz RX-sites 0 & 3 (ans 4 & 7) should be connected to the same optoboard.

The ribbons are assembled with a SMC-connector which fits into the SMC housind mounted on the BOC. Therefor the direction of ribbon is fixed on BOC side. The guiding pin is pointing away from BOC. On the Optoboard side the MT connector can be mounted in each direction. TX-board should be connected with the PiN on the optoboard, RX-board connected with the VCSELs on the optoboard.

1.2 Laser interlock

The interlock of the Back of Crate card consists of two signals. There is the local and the remote interlock signal. The local interlock will be set by the doorswitch to give an interlock if somebody is accessing the crate. The remote will be set by an ondetector interlock to switch lasers off if somebody is working on the opto components in the detector area.

For now the signals are to be switched directly on the crate, because there is no ondetector interlock signal. The two lines for the laser interlock on the BOC are switched between 5V and 0V. In case there is a backplane, one will find a 4 pin connector to connect a switching board. The signals are p1: 5V, p2: GND, p3: remote, p4: local.

In Wuppertal a small board has been developed to switch the interlocks independently. The interlock from the BOC is released if both interlock signal are released. The switching board has to be connected to 5V (connector pin 1), GND (pin2), remote (pin3), local (pin4). If there is no backplane, the interconnection between ROD and BOC has to be contacted at D11 and A21 to the remote or local interlock line on the switching board (pins 3,4) and pin1 is still 5V, pin2 GND. Green LEDs on the switching board are giving the laser off state, red LEDs indicate laser on.

1.3 Optoboard

Two types of optoboards are availabe, D-type (typically only one VCSEL array) and B-type optoboards (always two VCSEL arrays). The D-type optoboard is ment for use in the Disk/Layer 1 system. It is assembled with a PiN and one VCSEL array. This VCSELS are connected either to DTO or DTO2 of the MCC. Therefore it can be used for 40 Mbit/s and 80Mbit/s data transfer.
The B-type optoboard is for use in the B-Layer system. So it is made with a PiN and two VCSEL arrays. There are all DTO and DTO2 lines connected to the VCSELs and they are arranged modules wise. That's why these board is able to handle the 160 Mbit/s transfer speed which is in fact $2 \cdot 80\,Mbit/s$.
The optoboard is placed onto the PP0 (- support board). The PiN is connected via optical fibre ribbon to a TX plugin on the BOC card and the VCSELs are connected via optical fibre ribbon to a RX plugin on the BOC card each.
There are connectors for the Opto-Reset, the Opto-NTC and the powersupply on the PP0 support board.

The optoboard needs different voltages for operation:

$$\begin{aligned} V_{VDC} &= 2.5V \\ V_{PiN} &= 10V \\ V_{Iset} &\sim 0.8\ldots 1.0V \end{aligned} \tag{1.1}$$

There current comsumption for these voltages are:

$$\begin{aligned} V_{VDC}: I &= 220\,mA,\ (350\,mA \text{ for powered VCSELs}) \\ V_{PiN}: I &= 2\,mA - 10\,mA, \\ V_{Iset}: I &= 3\,mA. \end{aligned} \tag{1.2}$$

The current on the V_{PiN} is depending on the light power input the PiN. You should see there not less than $50\,\mu A$ per channel for a 50% high, 50% low signal. Normally the current is about $3.5\,mA$ for all channels together.

The MT8 ferule which is connected to the optoboard opto arrays has a degree of freedom in plugging it in. The assignment of the PiN or VCSEL channels to the modules connected to the PP0 you can find in the optoboard documentation (http://www.physics.ohio-state.edu/~gan/research.html, http://www.physics.ohio-state.edu/~rahimi/atlas/atlas.html). After switching on the Optoboard and switching on the light one has to reset the optoboard to have the propper 40 MHz clock. The minimal bending radius for the ribbons is 2cm.

Chapter 2

BocControl - the control program

2.1 Requirements and installation

You can get the program out of the CVS repository for the Pixel DAQ software. To operate the program the computer has to have installed the DataFlow and Online software in actual version, a QT in version ¿ 3.0 (for recompiling the program QT should have included the uspinbox from German Martinez (http://www.atlas.uni-wuppertal.de/ flick/uspinbox.tgz)), gcc 3.2, and the uspinbox files above mentioned. After downloading do a make in the program directory. Then execute the BocContol file.

2.2 A short manual

To set up the BOC for operation there is a QT-based tool: BocControl.

Prepare the system to be controlled:
In the main window (2.1) first you have to choose a slot in which the ROD/BOC pair is placed. By <Make Port> a software implementation of the ROD and BOC is created and you are able to talk to the BOC. With init BOC you set the BOC to defaults and initialize some important I2C chains. After this one can read back the status of BOC.

Ready to setup the BOC:
The <BocControl> button will open a window in which you find all the important settings to be controlled. There are three tabs containing the control for the clock (fig. 2.2), the RX- (fig. 2.3) and the TX-part (fig. 2.4).

The first tab (fig. 2.2) is providing the clock settings:
B-Clock setting should stay as it is, because it defines the phase between the ROD-clock and the module data going from the BOC to the ROD.

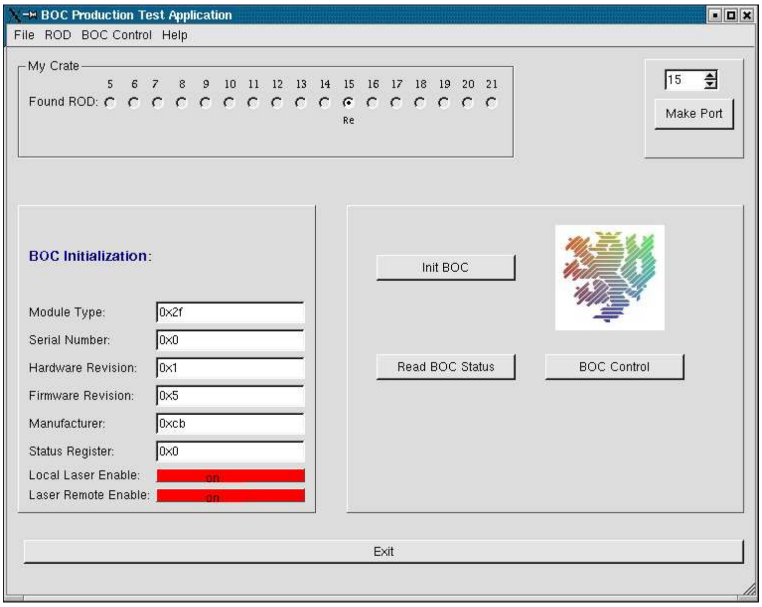

Figure 2.1: Main window of BocControl

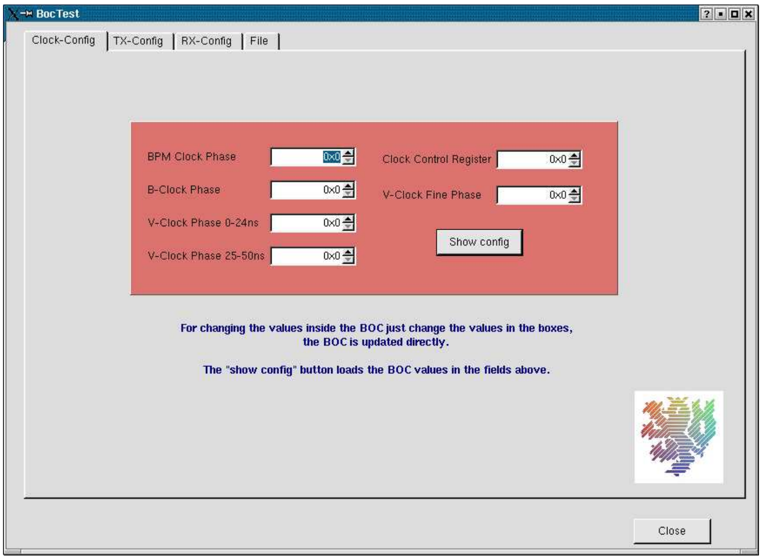

Figure 2.2: Clock tab of BocControl

BPM-Clock setting is controlling the delay of the clock which is going to the TX boards to be encoded in the BPM and sent to the modules. The V-Clock is important for splitting the 80MHz streams coming from the modules into two 40 MHz streams going to the ROD. It should be the inverted B-clock, perhaps tuned a bit.
Clock Control register settings are given in table 2.1. The delay steps are given in

Bits of Clock Control Register [4:0]	Functionality
0	V-clock invert
1	V-clock half
2	VernierStep bypass
3	BPM phase bypass
4	Phos4 divided by 4

Table 2.1: Values of the clock control register bits

Signal	Delay	Step	Range	hex
B-clock	B-clock delay	1ns	0..25ns	0x0..0x18
V-clock	V-clock delay 0	1ns	0..25ns	0x0..0x18
	V-clock delay 1	1ns	0..25ns	0x0..0x18
	V-clock fine delay	40ps	0..10.2ns	0x0..0xff
RX-Data	RX-Delay	1ns	0..25ns	0x0..0x18
TX-data	BPM fine delay	500 ps	0.. 63.5ns	0x0..7f
	BPM coarse delay	25ns	0..775ns	0x0..1f

Table 2.2: Delay settings for the different clocks

table 2.2, RX modes in table 2.3.

There are different modes to operate the BOC. They are accessible by setting the RX-Mode register. The values for the different modes are given in table 2.3.

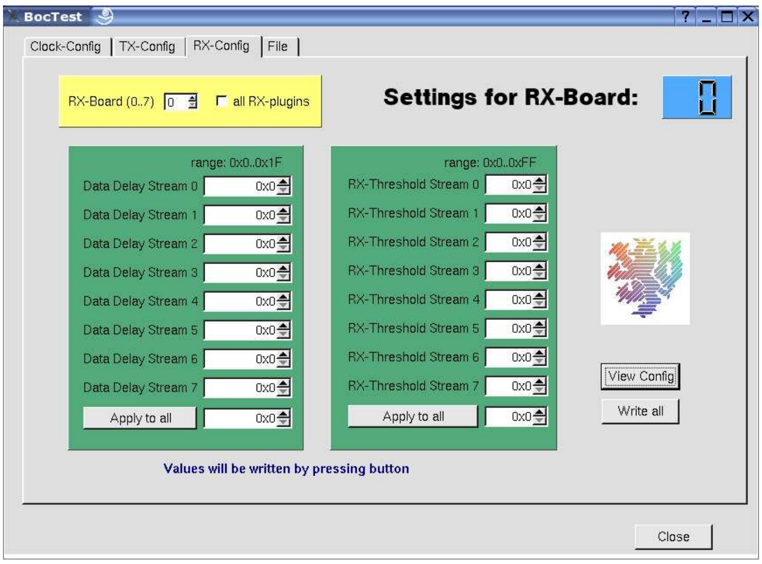

Figure 2.3: RX tab of BocControl

RX Mode	Action
0	Pixel Layer 2 (40Mb/s) remapped
1	Pixel B-Layer Mode (2*80Mb/s, Disk/L1 Optoboard, piggyback V1)
2	Pixel B-Layer Mode (2*80Mb/s, B-Layer Optoboard, piggyback V2)
3	Pixel B-Layer Mode (2*80Mb/s, B-Layer Optoboard, piggyback V2) AND Pixel DISK/L1 Mode (1*80Mb/s remapped, Disk/L1 optoboard, piggyback V2) so same as Mode 2, but EVEN/ODD BIT SWAPPED
4	phos clock test route 0
5	phos clock test route 1
6	CLOCK as DATA
7	TRANSPARENT MODE

Table 2.3: RX-Modes

The second tab (fig. 2.3) is providing the RX-settings. You can choose wether you want to talk to only one RX-board or all. The values which will be downloaded into the BOC are to be filled in the numeric fields. By pushing <Write All> all these values are written to the BOC. (Keep in mind, that only changing the values in the GUI is not updating the BOC.) Is the all RX-Boards checkbox checked. The values are written into all RX-boards (meaning values for stream 0 are written into the first stream for each RX-board and so on).

The same is valid for the third tab (fig. 2.4) where the TX-boards are controlled. Default values are 0x0 for all but Marks Space ration 0x13. The Mark Space Ratio of the BPM signal is influenced by the laser power and the fine delay setting. Changing these values can cause a signal which is not propper for the optoboard concerning the Mark Space Ratio which should be $50\% \pm 4\%$

The last tab provides the possibility to read in a config ascii file or to write the values which are present in the BOC registers to a file.

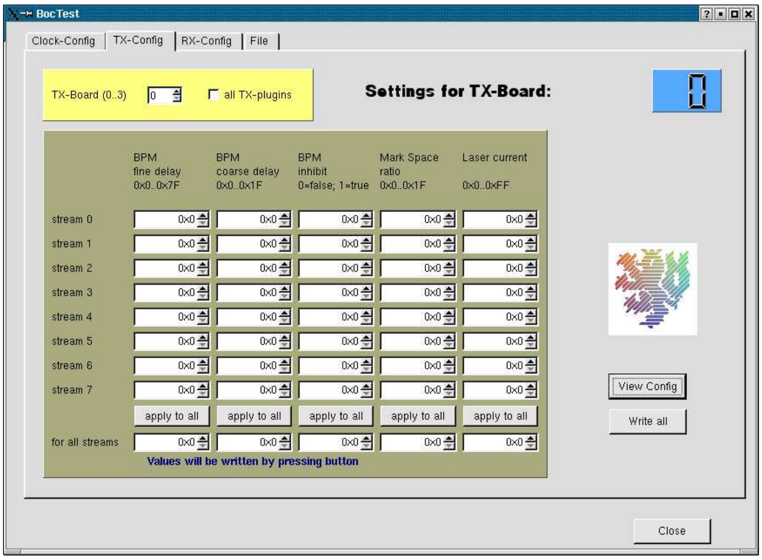

Figure 2.4: TX tab of BocControl